ESP32-S2

Datasheet

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Espressif System

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Product Overview

ESP32-S2 is a highly-integrated, low-power, 2.4 GHz Wi-Fi System-on-Chip (SoC) solution. With its state-of-the-art power and RF performance, this SoC is an ideal choice for a wide variety of application scenarios relating to Internet of Things (IoT), wearable electronics and smart home.

ESP32-S2 includes a Wi-Fi subsystem that integrates a Wi-Fi MAC, Wi-Fi radio and baseband, RF switch, RF balun, power amplifier, low noise amplifier (LNA), etc. The chip is fully compliant with the IEEE 802.11b/g/n protocol and offers a complete Wi-Fi solution.

At the core of this chip is an Xtensa® 32-bit LX7 CPU that operates at up to 240 MHz. The chip supports application development, without the need for a host MCU.

The on-chip memory includes 320 KB SRAM and 128 KB ROM. It also supports multiple external SPI/QSPI/OSPI flash and external RAM chips for more memory space.

ESP32-S2 is designed for ultra-low-power applications with its multiple low-power modes. Its featured fine-grained clock gating, dynamic voltage and frequency scaling, and adjustable power amplifier output power, contribute to an optimal trade-off between communication range, data rate and power consumption.

The device provides a rich set of peripheral interfaces including SPI, I^{2}S, UART, I^{2}C, LED_PWM, LCD interface, camera interface, ADC, DAC, touch sensor, temperature sensor, as well as 43 GPIOs. It also includes a full-speed USB On-The-Go (OTG) interface to enable USB communication.

ESP32-S2 has several dedicated hardware security features. Cryptographic accelerators are integrated for AES, SHA and RSA algorithms. Additional hardware security features are provided by the RNG, HMAC and Digital Signature modules as well as flash encryption and secure boot signature verification features. These features allow the device to meet stringent security requirements.

Block Diagram

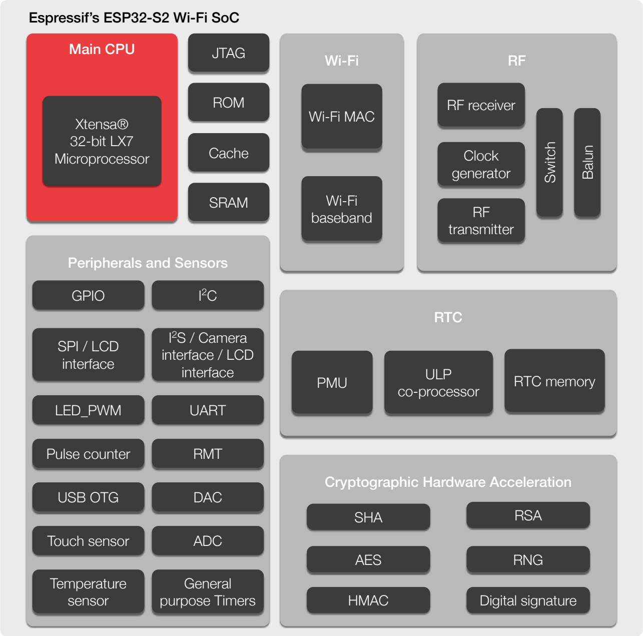

Figure 1: Block Diagram of ESP32-S2

Features

Wi-Fi

- IEEE 802.11 b/g/n-compliant
- Supports 20 MHz, 40 MHz bandwidth in 2.4 GHz band
- Single-band 1T1R mode with data rate up to 150 Mbps
- WMM
- TX/RX A-MPDU, RX A-MSDU
- Immediate Block ACK
- Fragmentation and defragmentation
- Automatic Beacon monitoring (hardware TSF)
- 4 × virtual Wi-Fi interfaces
- Simultaneous support for Infrastructure Station, SoftAP, and Promiscuous modes
  Note that when ESP32-S2 is in Station mode and performs a scan, the SoftAP channel will change along with the Station channel.
- Antenna diversity
- 802.11mc FTM

CPU and Memory

- Xtensa® single-core 32-bit LX7 microprocessor, up to 240 MHz
- 128 KB ROM
- 320 KB SRAM
- 16 KB SRAM in RTC
- SPI/QSPI/OSPI supports multiple flash and external RAM chips

Advanced Peripheral Interfaces

- 43 × programmable GPIOs
- 2 × 12-bit SAR ADCs, up to 20 channels
- 2 × 8-bit DAC
- 14 × touch sensing IOs
- 4 × SPI
- 1 × I²S
- 2 × I²C
- 2 × UART
- RMT (TX/RX)
- LED_PWM, up to 8 channels
- 1 × full-speed USB OTG
- 1 × temperature sensor
- 1 × DVP 8/16 camera interface, implemented using the hardware resources of I²S
- 1 × LCD interface (8-bit serial RGB/8080/6800), implemented using the hardware resources of SPI2
- 1 × LCD interface (8/16/24-bit parallel), implemented using the hardware resources of I²S

Security

- Secure boot
- Flash encryption
- 4096-bit OTP, up to 1792 bits for users
- Cryptographic hardware acceleration:
  - AES-128/192/256 (FIPS PUB 197)
  - Hash (FIPS PUB 180-4)
  - RSA
  - Random Number Generator (RNG)
  - HMAC
  - Digital signature

Applications (A Non-exhaustive List)

- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- Over-the-top (OTT) Devices
- USB Devices
- Speech Recognition
- Image Recognition
- Mesh Networks
- Home Automation
  - Light control
  - Smart plugs
  - Smart door locks
- Smart Buildings
  - Smart lighting
  - Energy monitoring
- Industrial Automation
  - Industrial wireless control
  - Industrial robotics
- Smart Agriculture
  - Smart greenhouses
  - Smart irrigation
  - Agriculture robotics
- Audio Applications
  - Internet music players
  - Live streaming devices
  - Internet radio players
  - Audio headsets
- Health Care Applications
  - Health monitoring
  - Baby monitors
- Wi-Fi-enabled Toys
  - Remote control toys
  - Proximity sensing toys
  - Educational toys
- Wearable Electronics
  - Smart watches
  - Smart bracelets
- Retail & Catering Applications
  - POS machines
  - Service robots
- Touch Sensing Applications
  - Waterproof design
  - Distance sensing applications
  - Linear slider, wheel slider designs

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1.1 Pin Layout

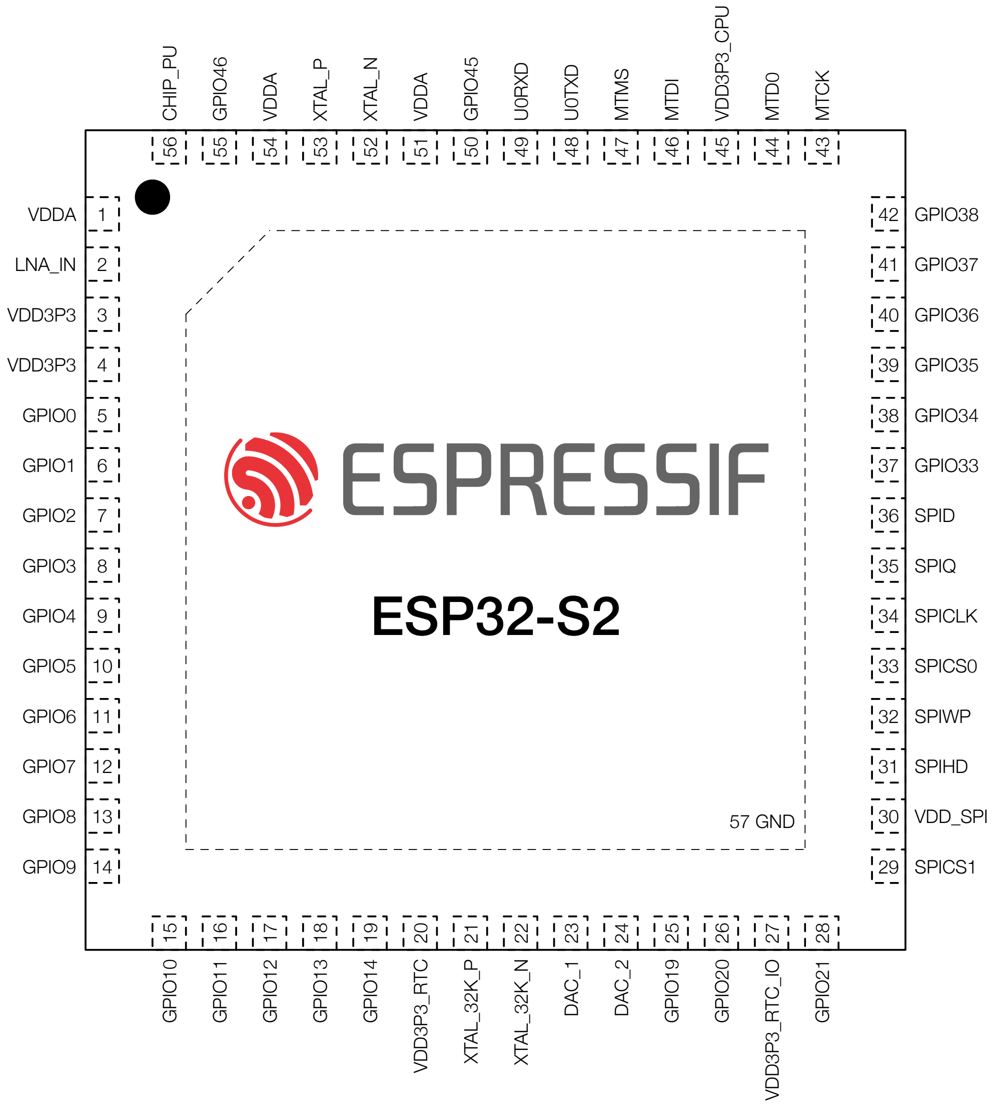


Figure 2: ESP32-S2 Pin Layout (Top View)

1.2 Pin Description

Table 1: Pin Description

Name	No.	Type	Power domain	Function
VDDA	1	P$_A$	—	Analog power supply
LNA_IN	2	I/O	—	RF input and output
VDD3P3	3	P$_A$	—	Analog power supply
VDD3P3	4	P$_A$	—	Analog power supply
GPIO0	5	I/O/T	VDD3P3_RTC_IO	RTC_GPIO0, GPIO0
GPIO1	6	I/O/T	VDD3P3_RTC_IO	RTC_GPIO1, GPIO1, TOUCH1, ADC1_CH0
GPIO2	7	I/O/T	VDD3P3_RTC_IO	RTC_GPIO2, GPIO2, TOUCH2, ADC1_CH1
GPIO3	8	I/O/T	VDD3P3_RTC_IO	RTC_GPIO3, GPIO3, TOUCH3, ADC1_CH2
GPIO4	9	I/O/T	VDD3P3_RTC_IO	RTC_GPIO4, GPIO4, TOUCH4, ADC1_CH3
GPIO5	10	I/O/T	VDD3P3_RTC_IO	RTC_GPIO5, GPIO5, TOUCH5, ADC1_CH4
GPIO6	11	I/O/T	VDD3P3_RTC_IO	RTC_GPIO6, GPIO6, TOUCH6, ADC1_CH5
GPIO7	12	I/O/T	VDD3P3_RTC_IO	RTC_GPIO7, GPIO7, TOUCH7, ADC1_CH6
GPIO8	13	I/O/T	VDD3P3_RTC_IO	RTC_GPIO8, GPIO8, TOUCH8, ADC1_CH7
GPIO9	14	I/O/T	VDD3P3_RTC_IO	RTC_GPIO9, GPIO9, TOUCH9, ADC1_CH8, FSPIHD
GPIO10	15	I/O/T	VDD3P3_RTC_IO	RTC_GPIO10, GPIO10, TOUCH10, ADC1_CH9, FSPICS0, FSPIIO4
GPIO11	16	I/O/T	VDD3P3_RTC_IO	RTC_GPIO11, GPIO11, TOUCH11, ADC2_CH0, FSPID, FSPIIO5
GPIO12	17	I/O/T	VDD3P3_RTC_IO	RTC_GPIO12, GPIO12, TOUCH12, ADC2_CH1, FSPICLK, FSPIIO6
GPIO13	18	I/O/T	VDD3P3_RTC_IO	RTC_GPIO13, GPIO13, TOUCH13, ADC2_CH2, FSPIQ, FSPIIO7
GPIO14	19	I/O/T	VDD3P3_RTC_IO	RTC_GPIO14, GPIO14, TOUCH14, ADC2_CH3, FSPIWP, FSPIDQS
VDD3P3_RTC	20	P$_A$	—	Analog power supply
XTAL_32K_P	21	I/O/T	VDD3P3_RTC_IO	RTC_GPIO15, GPIO15, U0RTS, ADC2_CH4, XTAL_32K_P
XTAL_32K_N	22	I/O/T	VDD3P3_RTC_IO	RTC_GPIO16, GPIO16, U0CTS, ADC2_CH5, XTAL_32K_N
DAC_1	23	I/O/T	VDD3P3_RTC_IO	RTC_GPIO17, GPIO17, U1TXD, ADC2_CH6, DAC_1
DAC_2	24	I/O/T	VDD3P3_RTC_IO	RTC_GPIO18, GPIO18, U1RXD, ADC2_CH7, DAC_2, CLK_OUT3

Name	No.	Type	Power domain	Function
GPIO19	25	I/O/T	VDD3P3_RTC_IO	RTC_GPIO19, GPIO19, U1RTS, ADC2_CH8, CLK_OUT2, USB_D-
GPIO20	26	I/O/T	VDD3P3_RTC_IO	RTC_GPIO20, GPIO20, U1CTS, ADC2_CH9, CLK_OUT1, USB_D+
VDD3P3_RTC_IO	27	P_D	VDD3P3_RTC_IO	Input power supply for RTC IO
GPIO21	28	I/O/T	VDD3P3_RTC_IO	RTC_GPIO21, GPIO21
SPICS1	29	I/O/T	VDD_SPI	SPICS1, GPIO26
VDD_SPI	30	P_D	—	Output power supply: 1.8 V or the same voltage as VDD3P3_RTC_IO
SPIHD	31	I/O/T	VDD_SPI	SPIHD, GPIO27
SPIWP	32	I/O/T	VDD_SPI	SPIWP, GPIO28
SPICS0	33	I/O/T	VDD_SPI	SPICS0, GPIO29
SPICLK	34	I/O/T	VDD_SPI	SPICLK, GPIO30
SPIQ	35	I/O/T	VDD_SPI	SPIQ, GPIO31
SPID	36	I/O/T	VDD_SPI	SPID, GPIO32
GPIO33	37	I/O/T	VDD3P3_CPU / VDD_SPI	SPIIO4, GPIO33, FSPIHD
GPIO34	38	I/O/T	VDD3P3_CPU / VDD_SPI	SPIIO5, GPIO34, FSPICS0
GPIO35	39	I/O/T	VDD3P3_CPU / VDD_SPI	SPIIO6, GPIO35, FSPID
GPIO36	40	I/O/T	VDD3P3_CPU / VDD_SPI	SPIIO7, GPIO36, FSPICLK
GPIO37	41	I/O/T	VDD3P3_CPU / VDD_SPI	SPIDQS, GPIO37, FSPIQ
GPIO38	42	I/O/T	VDD3P3_CPU	GPIO38, FSPIWP
MTCK	43	I/O/T	VDD3P3_CPU	MTCK, GPIO39, CLK_OUT3
MTDO	44	I/O/T	VDD3P3_CPU	MTDO, GPIO40, CLK_OUT2
VDD3P3_CPU	45	P_D	—	Input power supply for CPU IO
MTDI	46	I/O/T	VDD3P3_CPU	MTDI, GPIO41, CLK_OUT1
MTMS	47	I/O/T	VDD3P3_CPU	MTMS, GPIO42
U0TXD	48	I/O/T	VDD3P3_CPU	U0TXD, GPIO43, CLK_OUT1
U0RXD	49	I/O/T	VDD3P3_CPU	U0RXD, GPIO44, CLK_OUT2
GPIO45	50	I/O/T	VDD3P3_CPU	GPIO45
VDDA	51	P_A	—	Analog power supply
XTAL_N	52	—	—	External crystal output

Name	No.	Type	Power domain	Function
XTAL_P	53	—	—	External crystal input
VDDA	54	P_A	—	Analog power supply
GPIO46	55	I	VDD3P3_CPU	GPIO46
CHIP_PU	56	I	VDD3P3_RTC_IO	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the CHIP_PU pin floating.
GND	57	G	—	Ground

Note:

1. P: power pin; I: input; O: output; T: high impedance.
2. ESP32-S2's pins SPICS1, SPIHD, SPIWP, SPICS0, SPICLK, SPIQ and SPID are usually used for connecting the embedded flash and external RAM, and are not recommended for other uses.
3. For the data port connection between ESP32-S2 and external flash please refer to Section 2.4.2.
4. Power supply for GPIO33, GPIO34, GPIO35, GPIO36 and GPIO37 is configurable to be either VDD3P3_CPU (default) or VDD_SPI.
5. The pin function in this table refers only to some fixed settings and do not cover all cases for signals that can be input and output through the GPIO matrix. For more information on the GPIO matrix, please refer to Table 15.

1.3 Power Scheme

ESP32-S2's digital pins are divided into four different power domains:

- VDD3P3_RTC_IO
- VDD3P3_CPU
- VDD_SPI
- VDD3P3_RTC

VDD3P3_RTC_IO is the input power supply for RTC and CPU.

VDD3P3_CPU is the input power supply for CPU.

VDD_SPI can be an input power supply or an output power supply. VDD_SPI connects to the output of an internal LDO whose input is VDD3P3_RTC_IO. When VDD_SPI is connected to the same PCB net together with VDD3P3_RTC_IO, the internal LDO should be disabled.

VDD3P3_RTC is the input power supply for RTC analog.

The power scheme diagram is shown in Figure 3.

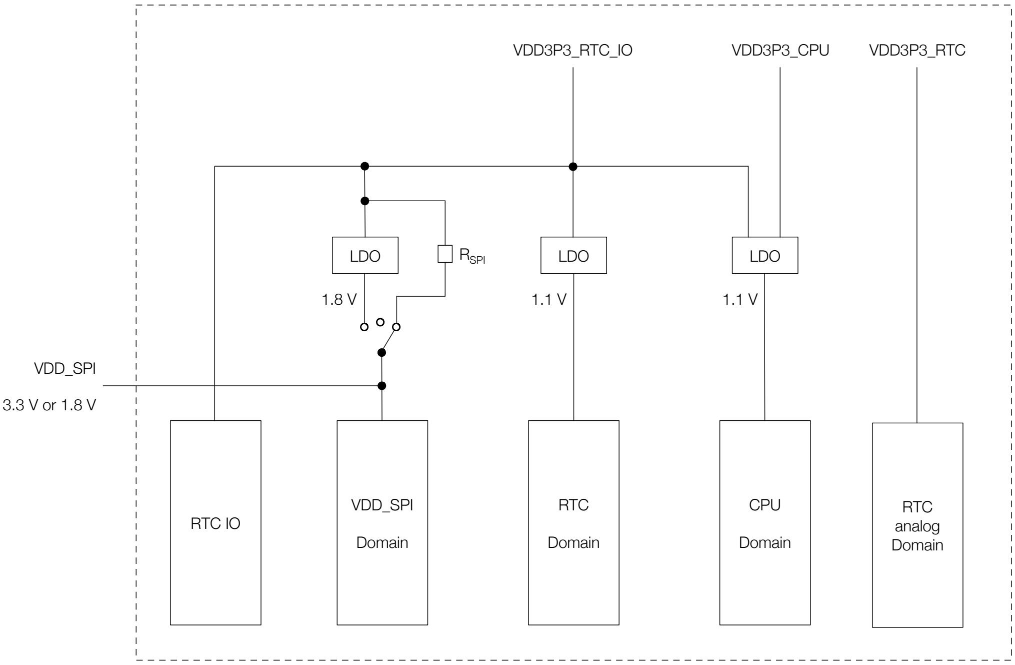


Figure 3: ESP32-S2 Power Scheme

The VDD_SPI voltage can be configured at 1.8 V using an internal LDO, or powered by VDD3P3_RTC_IO via R$_{SPI}$ (nominal 3.3 V). The VDD_SPI can be powered off via software to minimize the current leakage of flash in the Deep-sleep mode.

Notes on CHIP_PU:

The illustration below shows the ESP32-S2 power-up and reset timing. Details about the parameters are listed in Table 2.

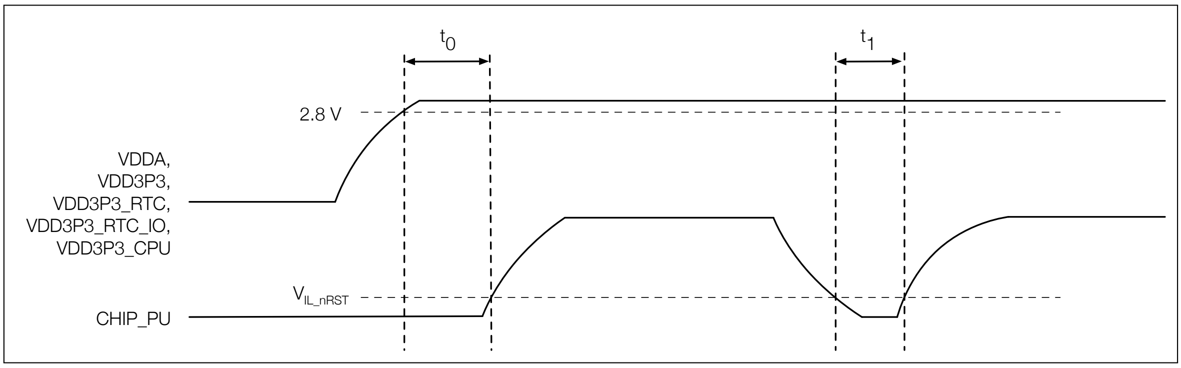


Figure 4: ESP32-S2 Power-up and Reset Timing

Table 2: Description of ESP32-S2 Power-up and Reset Timing Parameters

Parameters	Description	Min.	Unit
t_0	Time between bringing up the VDDA, VDD3P3, VDD3P3_RTC, VDD3P3_RTC_IO and VDD3P3_CPU rails, and activating CHIP_PU.	0.5	ms
t_1	Duration of CHIP_PU signal level < V_{IL_nRST} (refer to its value in Table 9 DC Characteristics) to reset the chip.	0.5	ms

1.4 Strapping Pins

ESP32-S2 has three strapping pins:

- GPIO0
- GPIO45
- GPIO46

Software can read the values of corresponding bits from register ”GPIO_STRAPPING”.

During the chip’s system reset (power-on-reset, RTC watchdog reset, brownout reset, analog super watchdog reset, and crystal clock glitch detection reset), the latches of the strapping pins sample the voltage level as strapping bits of ”0” or ”1”, and hold these bits until the chip is powered down or shut down.

GPIO0, GPIO45 and GPIO46 are connected to the chip’s internal pull-up/pull-down during the chip reset. Consequently, if they are unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of these strapping pins.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU’s GPIOs to control the voltage level of these pins when powering on ESP32-S2.

After reset, the strapping pins work as normal-function pins.

Refer to Table 3 for a detailed boot-mode configuration of the strapping pins.

Table 3: Strapping Pins

VDD_SPI Voltage [1]			
Pin	Default	3.3 V	1.8 V
GPIO45	Pull-down	0	1
Booting Mode [2]			

Pin	Default	SPI Boot	Download Boot
GPIO0	Pull-up	1	0
GPIO46	Pull-down	Don't-care	0
Enabling/Disabling ROM Code Print During Booting [3] [4]			
Pin	Default	Enabled	Disabled
GPIO46	Pull-down	See the fourth note	See the fourth note

Note:

1. The functionality of strapping pin GPIO45 to select VDD_SPI voltage may be disabled by setting VDD_SPI_FORCE eFuse to 1. In such a case the voltage is selected with eFuse bit VDD_SPI_TIEH.
2. The strapping combination of GPIO46 = 1 and GPIO0 = 0, or GPIO46 = 0 and GPIO0 = 1 is invalid and will trigger unexpected behavior.
3. ROM code can be printed over U0TXD (by default) or DAC_1, depending on the eFuse bit.
4. When eFuse UART_PRINT_CONTROL value is:
   0, print is normal during boot and not controlled by GPIO46.
   1 and GPIO46 is 0, print is normal during boot; but if GPIO46 is 1, print is disabled.
   2 and GPIO46 is 0, print is disabled; but if GPIO46 is 1, print is normal.
   3, print is disabled and not controlled by GPIO46.

2. Functional Description

This chapter describes the functions of ESP32-S2.

2.1 CPU and Memory

2.1.1 CPU

ESP32-S2 contains one low-power Xtensa® 32-bit LX7 microprocessor with the following features:

- 7-stage pipeline that supports the clock frequency of up to 240 MHz
- 16/24-bit Instruction Set providing high code-density
- support for 32-bit multiplier and 32-bit divider
- unbuffered GPIO instructions
- support for 32 interrupts at six levels
- support for windowed ABI with 64 physical general registers
- support for trace function with TRAX compressor, up to 16 KB trace memory
- JTAG for debugging

2.1.2 Internal Memory

ESP32-S2's internal memory includes:

- **128 KB of ROM**: for booting and core functions
- **320 KB of on-chip SRAM**: for data and instructions
- **8 KB of SRAM in RTC**: called RTC FAST Memory and can be accessed by the main CPU. It can retain data in Deep-sleep mode.
- **RTC SLOW Memory**: it can be accessed by the main CPU or the co-processor. It can retain data in Deep-sleep mode.
- **4 Kbit of eFuse**: 1792 bits are reserved for user data, such as encryption key and device ID.

2.1.3 External Flash and RAM

ESP32-S2 supports multiple external QSPI/OSPI flash and RAM chips. It also supports hardware encryption/decryption based on XTS-AES to protect developers' programs and data in flash and RAM.

The external flash and RAM can be mapped into the CPU instruction memory space and read-only data memory space. The RAM can also be mapped into the CPU data memory space. Up to 1 GB of external flash and RAM can be supported.

Through high-speed caches, ESP32-S2 can support the following mappings at the same time.

- Up to 7.5 MB of instruction memory space can be mapped at a time into flash and RAM. If more than 3.5 MB are mapped, cache performance may be slightly reduced due to the CPU's pipeline characteristics.
- Up to 4 MB of read-only data memory space can be mapped into flash or RAM as individual 64 KB blocks. 8-bit, 16-bit and 32-bit reads are supported.

- Up to 10.5 MB of read-write data memory space can be mapped into RAM as individual 64 KB blocks. 8-bit, 16-bit and 32-bit reads and writes are supported. Blocks from this 10.5 MB space can also be mapped into flash, for read operations only.

> **Note:**
> After ESP32-S2 is initialized, firmware can customize the mapping of external RAM or flash into the CPU address space.

2.1.4 Address Mapping Structure

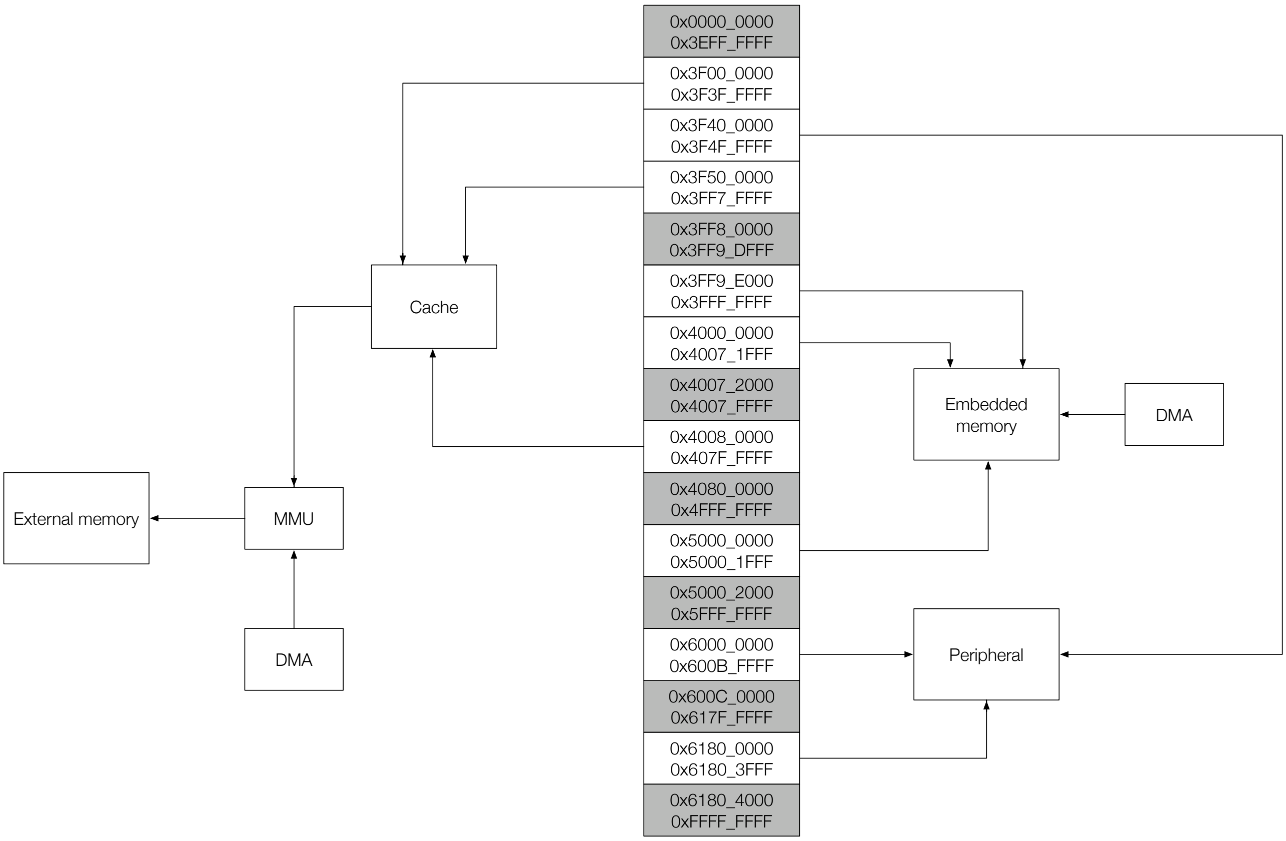


Figure 5: Address Mapping Structure

> **Note:**
> The memory space with gray background is not available to users.

2.1.5 Cache

ESP32-S2 has independent instruction Cache and data Cache that have the following features:

- configurable size of 8 KB or 16 KB
- 4-channel group association
- block size of 16 bytes or 32 bytes
- pre-load function
- lock function

- support for critical word first and early restart

2.2 System Clocks

2.2.1 CPU Clock

The CPU clock has four possible sources:

- external 40 MHz crystal clock
- internal 8 MHz oscillator
- PLL clock
- audio PLL clock

The application can select the clock source from the external crystal clock source, the PLL clock, the audio PLL clock, or the internal 8 MHz oscillator. The selected clock source drives the CPU clock directly, or after division, depending on the application.

2.2.2 RTC Clock

The RTC slow clock has three possible sources:

- external low-speed (32 kHz) crystal clock
- internal RC oscillator (typically about 150 kHz, and adjustable)
- internal 31.25 kHz clock (derived from the internal 8 MHz oscillator divided by 256)

The RTC fast clock has two possible sources:

- external crystal clock divided by 4
- internal 8 MHz oscillator

The RTC slow clock is used for RTC counter, RTC watchdog and low-power controller; while the RTC fast clock for RTC peripherals and sensing controllers.

2.2.3 Audio PLL Clock

The audio clock is generated by the low-noise fractional-N PLL.

2.3 Analog Peripherals

2.3.1 Analog-to-Digital Converter (ADC)

ESP32-S2 integrates two 12-bit SAR ADCs and supports measurements on 20 channels (analog-enabled pins). The ULP-coprocessor in ESP32-S2 is also designed to measure voltage. The ULP can operate while the main CPU is in Deep-sleep mode, which lowers the total power consumption. By using threshold settings, and / or via other triggers or events, we can interrupt the CPU from the sleep state.

The ADCs can be configured to measure voltage on up to 20 pins.

For ADC characteristics, please refer to Table 10.

2.3.2 Digital-to-Analog Converter (DAC)

ESP32-S2 has two 8-bit DAC channels that convert two digital signals into two analog voltage signal outputs. The two DAC channels support independent conversions. The design structure is composed of integrated resistor strings and a buffer. This dual DAC supports VDD3P3_RTC_IO power supply as input voltage reference.

2.3.3 Temperature Sensor

The temperature sensor generates a voltage that varies with temperature. The voltage is internally converted via an ADC into a digital value.

The temperature sensor has a range of –20 °C to 110 °C. It is designed primarily to sense the temperature changes inside the chip. The temperature value depends on factors like microcontroller clock frequency or I/O load. Generally, the chip's internal temperature is higher than the ambient temperature.

2.3.4 Touch Sensor

ESP32-S2 has 14 capacitive-sensing GPIOs, which detect variations induced by touching or approaching the GPIOs with a finger or other objects. The low-noise nature of the design and the high sensitivity of the circuit allow relatively small pads to be used. Arrays of pads can also be used, so that a larger area or more points can be detected. The touch sensing performance can be further enhanced by the waterproof design and digital filtering feature. The 14 capacitive-sensing GPIOs are listed in Table 4.

Table 4: Capacitive-Sensing GPIOs Available on ESP32-S2

Capacitive-sensing signal name	Pin name
TOUCH1	GPIO1
TOUCH2	GPIO2
TOUCH3	GPIO3
TOUCH4	GPIO4
TOUCH5	GPIO5
TOUCH6	GPIO6
TOUCH7	GPIO7
TOUCH8	GPIO8
TOUCH9	GPIO9
TOUCH10	GPIO10
TOUCH11	GPIO11
TOUCH12	GPIO12
TOUCH13	GPIO13
TOUCH14	GPIO14

2.4 Digital Peripherals

2.4.1 General Purpose Input / Output Interface (GPIO)

ESP32-S2 has 43 GPIO pins which can be assigned various functions by programming the appropriate registers. Some GPIOs can be used both for digital signals but also for analog functions, such as ADC, DAC and touch sensing.

All GPIOs can be configured as internal pull-up or pull-down, or set to high impedance, except for GPIO46, which is fixed to pull-down. When configured as an input, the input value can be read by software through the register. The input can also be set to edge-trigger or level-trigger to generate CPU interrupts. Except for GPIO46 (input only), all digital IO pins are bi-directional, non-inverting and tristate, including input and output buffers with tristate control. These pins can be multiplexed with other functions, such as the UART, SPI, etc. For low-power operations, the GPIOs can be set to hold their states.

2.4.2 Serial Peripheral Interface (SPI)

ESP32-S2 features four SPI interfaces (SPI0, SPI1, SPI2 and SPI3). SPI0 and SPI1 can only be configured to operate in SPI memory mode; SPI2 can be configured to operate in SPI memory and general-purpose SPI modes; SPI3 can only be configured to operate in general-purpose SPI mode.

- **SPI Memory mode**

  In SPI memory mode, SPI0, SPI1 and SPI2 interface with external SPI memory. Data transmission is in multiples of bytes. Up to 8-line STR/DDR reads and writes are supported. The clock frequency is configurable to a maximum of 80 MHz in STR mode and a maximum of 40 MHz in DDR mode.

- **SPI2 General-purpose SPI (GP-SPI) mode**

  When SPI2 acts as a general-purpose SPI, it can operate in master and slave modes. The master mode supports 2-line full-duplex communication and 1-/2-/4-/8-line half-duplex communication. The slave mode supports 2-line full-duplex communication and 1-/2-/4-line half-duplex communication. The host's clock frequency is configurable. Data transmission is in multiples of bytes. The clock polarity (CPOL) and phase (CPHA) are also configurable. The SPI2 interface supports DMA.

  - In 2-line full-duplex communication mode, the host's clock frequency is configurable to 80 MHz at most, and the slave's clock frequency to 40 MHz at most. Four modes of SPI transfer format are supported.
  - In 1-/2-/4-/8-line half-duplex communication mode, the host's clock frequency is configurable to 80 MHz at most and the four modes of SPI transfer format are supported.
  - In 1-/2-/4-line half-duplex communication mode, the slave's clock frequency is configurable to 40 MHz at most, and the four modes of SPI transfer format are also supported.

- **SPI3 General-purpose SPI (GP-SPI) mode**

  As a general-purpose SPI interface, SPI3 can operate in master and slave modes, in 2-line full-duplex and 1-line half-duplex communication modes. The host's clock frequency is configurable. Data transmission is in multiples of bytes. The clock polarity (CPOL) and phase (CPHA) are also configurable. The SPI3 interface supports DMA.

  - In 2-line full-duplex communication mode, the host's clock frequency is configurable to a maximum of 80 MHz, and the slave's clock frequency to 40 MHz at most. Four modes of SPI transfer format are supported.

  - In 1-line half-duplex communication mode, the host's clock frequency is configurable to a maximum of 80 MHz, and the slave's clock frequency to 40 MHz at most. The four modes of SPI transfer format are supported.

In most cases, the data port connection between ESP32-S2 and external flash is as follows:

SPI 8-line mode:

- SPID (SPID) = IO0
- SPIQ (SPIQ) = IO1
- SPIWP (SPIWP) = IO2
- SPIHD (SPIHD) = IO3
- GPIO33 = IO4
- GPIO34 = IO5
- GPIO35 = IO6
- GPIO36 = IO7
- GPIO37 = DQS

SPI 4-line mode:

- SPID (SPID) = IO0
- SPIQ (SPIQ) = IO1
- SPIWP (SPIWP) = IO2
- SPIHD (SPIHD) = IO3

SPI 2-line mode:

- SPID (SPID) = IO0
- SPIQ (SPIQ) = IO1

SPI 1-line mode:

- SPIQ (SPIQ) = DO
- SPID (SPID) = DI
- SPIHD (SPIHD) = HOLD#
- SPIWP (SPIWP) = WP#

2.4.3 LCD Interface

The LCD interface supports 8-bit serial RGB, 8080 and 6800 modes. It is implemented using the hardware resources of SPI2. The LCD interface can also support 8/16/24-bit parallel interface (8080), implemented using the hardware resources of I^{2}S.

2.4.4 Universal Asynchronous Receiver Transmitter (UART)

ESP32-S2 has two UART interfaces, i.e., UART0, UART1, which provide asynchronous communication (RS232 and RS485) and IrDA support, communicating at a speed of up to 5 Mbps. UART provides hardware management of the CTS and RTS signals and software flow control (XON and XOFF). All of the interfaces can be accessed by the DMA controller or directly by the CPU.

2.4.5 I²C Interface

ESP32-S2 has two I²C bus interfaces which can serve as I²C master or slave, depending on the user's configuration. The I²C interfaces support:

- standard mode (100 Kbit/s)
- fast mode (400 Kbit/s)
- up to 5 MHz (constrained by SDA pull-up strength)
- 7-bit/10-bit addressing mode
- dual addressing mode

Users can program command registers to control I²C interfaces, so that they have more flexibility.

2.4.6 I²S Interface

ESP32-S2 includes a standard I²S interface. It can operate in master or slave mode, in full-duplex and half-duplex communication modes, and can be configured to operate with an 8-/16-/24-/32-/48-/64-bit resolution as an input or output channel. BCK clock frequency, from 10 kHz up to 40 MHz, is supported.

The I²S interface has a dedicated DMA controller. PCM interface is supported.

2.4.7 Camera Interface

ESP32-S2 supports one 8 or 16-bit DVP image sensor, with clock frequency of up to 40 MHz. The camera interface is implemented by using the hardware resources of I²S.

2.4.8 Infrared Remote Controller

The infrared remote controller supports four channels of infrared remote transmission and reception. By programming the pulse waveform, it supports various infrared and other single wire protocols. Four channels share a 256 × 32-bit block of memory to store the transmitting or receiving waveform.

2.4.9 Pulse Counter

The pulse counter captures pulse and counts pulse edges through multiple modes. It has four channels, each of which captures four signals at a time. The four input signals include two pulse signals and two control signals.

2.4.10 LED_PWM

The LED_PWM controller can generate eight independent channels. The LED_PWM controller:

- can generate digital waveforms with configurable periods and duties. The accuracy of duty can be up to 18 bits within a 1 ms period.
- has multiple clock sources, including APB clock and external crystal clock.
- can operate when the CPU is in Light-sleep mode.

- supports gradual increase or decrease of duty cycle, which is useful for the LED RGB color-gradient generator.

2.4.11 USB 1.1 OTG

ESP32-S2 features a full-speed USB OTG interface which is compliant with the USB 1.1 specification. It has the following features:

- software-configurable endpoint settings and suspend/resume
- support for dynamic FIFO sizing
- support for session request protocol (SRP) and host negotiation protocol (HNP)
- a full-speed USB PHY integrated in the chip

2.5 Radio and Wi-Fi

The ESP32-S2 radio consists of the following blocks:

- 2.4 GHz receiver
- 2.4 GHz transmitter
- Bias and regulators
- Balun and transmit-receive switch
- Clock generator

2.5.1 2.4 GHz Receiver

The 2.4 GHz receiver demodulates the 2.4 GHz RF signal to quadrature baseband signals and converts them to the digital domain with two high-resolution, high-speed ADCs. To adapt to varying signal channel conditions, RF filters, Automatic Gain Control (AGC), DC offset cancelation circuits and baseband filters are integrated with ESP32-S2.

2.5.2 2.4 GHz Transmitter

The 2.4 GHz transmitter modulates the quadrature baseband signals to the 2.4 GHz RF signal, and drives the antenna with a high-powered Complementary Metal Oxide Semiconductor (CMOS) power amplifier. The use of digital calibration further improves the linearity of the power amplifier.

Additional calibrations are integrated to cancel any radio imperfections, such as:

- carrier leakage
- I/Q amplitude/phase matching
- baseband nonlinearities
- RF nonlinearities
- antenna matching

These built-in calibration routines reduce the cost, time, and specialized equipment required for product testing, and certification.

2.5.3 Clock Generator

The clock generator produces quadrature clock signals of 2.4 GHz for both the receiver and the transmitter. All components of the clock generator are integrated into the chip, including all inductors, varactors, filters, regulators and dividers.

The clock generator has built-in calibration and self-test circuits. Quadrature clock phases and phase noise are optimized on-chip with patented calibration algorithms which ensure the best performance of the receiver and the transmitter.

2.5.4 Wi-Fi Radio and Baseband

The ESP32-S2 Wi-Fi radio and baseband support the following features:

- 802.11b/g/n
- 802.11n MCS0-7 that supports 20 MHz and 40 MHz bandwidth
- 802.11n MCS32
- 802.11n 0.4 μs guard-interval
- single stream, data rate up to 150 Mbps
- STBC RX (Single spatial stream)
- adjustable transmitting power
- antenna diversity;
  ESP32-S2 supports antenna diversity with an external RF switch. One or more GPIOs control the RF switch and select the best antenna to minimize the effects of channel imperfections.

2.5.5 Wi-Fi MAC

ESP32-S2 implements the full 802.11 b/g/n Wi-Fi MAC protocol. It supports the Basic Service Set (BSS) STA and SoftAP operations under the Distributed Control Function (DCF). Power management is handled automatically with minimal host interaction to minimize the active-duty period.

The ESP32-S2 Wi-Fi MAC applies low-level protocol functions automatically. They are as follows:

- 4 × virtual Wi-Fi interfaces
- simultaneous Infrastructure BSS Station mode/SoftAP mode/Promiscuous mode
- RTS protection, CTS protection, Immediate Block ACK
- fragmentation and defragmentation
- TX/RX A-MPDU, RX A-MSDU
- TXOP
- WMM
- CCMP, TKIP, WAPI, WEP, BIP
- automatic beacon monitoring (hardware TSF)
- 802.11mc FTM

2.5.6 Networking Features

Users are provided with libraries for TCP/IP networking, ESP-MESH networking, and other networking protocols over Wi-Fi. TLS 1.0, 1.1 and 1.2 support is also provided.

2.6 RTC and Low-Power Management

2.6.1 Power Management Unit (PMU)

With the use of advanced power-management technologies, ESP32-S2 can switch between different power modes.

- Active mode: CPU and chip radio are powered on. The chip can receive, transmit, or listen.
- Modem-sleep mode: The CPU is operational and the clock speed can be reduced. The Wi-Fi baseband and radio are disabled, but Wi-Fi connection can remain active.
- Light-sleep mode: The CPU is paused. The RTC peripherals, as well as the ULP co-processor are running. Any wake-up events (MAC, host, RTC timer, or external interrupts) will wake up the chip. Wi-Fi connection can remain active.
- Deep-sleep mode: Only the RTC memory and RTC peripherals are powered on. Wi-Fi connection data are stored in the RTC memory. The ULP co-processor is functional.
- Hibernation mode: The internal 8-MHz oscillator and ULP co-processor are disabled. The RTC recovery memory is powered down. Only one RTC timer on the slow clock and certain RTC GPIOs are active. The RTC timer or the RTC GPIOs can wake up the chip from the Hibernation mode.

For power consumption in different power modes, please refer to Table 12.

2.6.2 Ultra-Low-Power Co-processor

The ULP co-processor is designed as a simplified, low-power replacement of CPU in sleep modes. It can be also used to supplement the functions of the CPU in normal working mode. The ULP co-processor and RTC memory remain powered on during the Deep-sleep mode. Hence, the developer can store a program for the ULP co-processor in the RTC slow memory to access RTC GPIO, RTC peripheral devices, RTC timers and internal sensors during the Deep-sleep mode.

ESP32-S2 has two ULP co-processors, with one based on RISCV instruction set architecture (ULP-RISCV) and the other on finite state machine (ULP-FSM).

ULP-RISCV has the following features:

- support for IMC instruction set
- thirty-two 32-bit general-purpose registers
- 32-bit multiplier and divider
- support for interrupts
- boot by the CPU, its dedicated timer, or RTC GPIO

ULP-FSM has the following features:

- support for common instructions including arithmetic, jump, and program control instructions
- support for on-board sensor measurement instructions

- boot by the CPU, its dedicated timer, or RTC GPIO

Note that these two co-processors cannot work simultaneously.

2.7 Timers and Watchdogs

2.7.1 64-bit Timers

There are four general-purpose timers embedded in ESP32-S2. They are all 64-bit generic timers which are based on 16-bit prescalers and 64-bit auto-reload-capable up/down-timers.

The timers' features are summarized as follows:

- a 16-bit clock prescaler, from 1 to 65536
- a 64-bit time-base counter programmable to be incrementing or decrementing
- able to read real-time value of the time-base counter
- halting and resuming the time-base counter
- programmable alarm generation
- timer value reload (Auto-reload at alarm or software-controlled instant reload)
- level and edge interrupt generation

2.7.2 Watchdog Timers

The ESP32-S2 contains three watchdog timers: one in each of the two timer groups (called Main System Watchdog Timers, or MWDT) and one in the RTC Module (called the RTC Watchdog Timer, or RWDT). Each watchdog timer allows for four separately configurable stages and each stage can be programmed to take one of three (or four for RWDT) actions upon expiry, unless the watchdog is fed or disabled. The actions upon expiry are: interrupt, CPU reset, core reset and system reset. Only RWDT can trigger a system reset that will reset the entire digital circuits, which is the main system including the RTC itself. A timeout value can be set for each stage individually.

During the flash boot process, RWDT and the first MWDT are enabled automatically in order to detect and recover from booting errors.

Watchdog timers have the following features:

- four stages, each with a programmable timeout value. Each stage can be configured and enabled/disabled separately
- one of three/four (for MWDTs/ RWDT) possible actions (interrupt, CPU reset, core reset and system reset) available upon expiry of each stage
- 32-bit expiry counter
- write protection, to prevent RWDT and MWDT configuration from being altered inadvertently
- flash boot protection
  If the boot process from an SPI flash does not complete within a predetermined period of time, the watchdog will reboot the entire main system.

2.8 Cryptographic Hardware Accelerators

ESP32-S2 is equipped with hardware accelerators of general algorithms, such as AES (FIPS PUB 197), ECB/CBC/OFB/CFB/CTR (NIST SP 800-38A), GCM (NIST SP 800-38D), SHA (FIPS PUB 180-4), RSA, and ECC, which support independent arithmetic, such as Big Integer Multiplication and Big Integer Modular Multiplication. The maximum operation length for RSA, Big Integer Multiplication and Big Integer Modular Multiplication is 4096 bits. The maximum factor length for Big Integer Multiplication is 2048 bits.

2.9 Physical Security Features

- Transparent external flash and RAM encryption (AES-XTS) with software inaccessible key prevents unauthorized readout of user application code or data.
- Secure Boot feature uses a hardware root of trust to ensure only signed firmware (with RSA-PSS signature) can be booted.
- HMAC module can use a software inaccessible MAC key to generate SHA-HMAC signatures for identity verification, as well as other uses.
- Digital Signature module can use a software inaccessible secure key to generate MAC signatures for identity verification.

2.10 Peripheral Pin Configurations

Table 5: Peripheral Pin Configurations

Interface	Signal	Pin	Function
ADC	ADC1_CH0	GPIO1	Two 12-bit SAR ADCs
	ADC1_CH1	GPIO2	
	ADC1_CH2	GPIO3	
	ADC1_CH3	GPIO4	
	ADC1_CH4	GPIO5	
	ADC1_CH5	GPIO6	
	ADC1_CH6	GPIO7	
	ADC1_CH7	GPIO8	
	ADC1_CH8	GPIO9	
	ADC1_CH9	GPIO10	
	ADC2_CH0	GPIO11	
	ADC2_CH1	GPIO12	
	ADC2_CH2	GPIO13	
	ADC2_CH3	GPIO14	
	ADC2_CH4	XTAL_32K_P	
	ADC2_CH5	XTAL_32K_N	
	ADC2_CH6	DAC_1	
	ADC2_CH7	DAC_2	
	ADC2_CH8	GPIO19	
	ADC2_CH9	GPIO20	

Interface	Signal	Pin	Function
DAC	DAC_1	DAC_1	Two 8-bit DACs
	DAC_2	DAC_2	
Touch sensor	TOUCH1	GPIO1	Capacitive touch sensors
	TOUCH2	GPIO2	
	TOUCH3	GPIO3	
	TOUCH4	GPIO4	
	TOUCH5	GPIO5	
	TOUCH6	GPIO6	
	TOUCH7	GPIO7	
	TOUCH8	GPIO8	
	TOUCH9	GPIO9	
	TOUCH10	GPIO10	
	TOUCH11	GPIO11	
	TOUCH12	GPIO12	
	TOUCH13	GPIO13	
	TOUCH14	GPIO14	
JTAG	MTDI	MTDI	JTAG for software debugging
	MTCK	MTCK	
	MTMS	MTMS	
	MTDO	MTDO	
UART	U0RXD_in	Any GPIO pins	Two UART devices with hardware flow-control and DMA
	U0CTS_in		
	U0DSR_in		
	U0TXD_out		
	U0RTS_out		
	U0DTR_out		
	U1RXD_in		
	U1CTS_in		
	U1TXD_out		
	U1RTS_out		
I^{2}C	I2CEXT0_SCL_in	Any GPIO pins	Two I^{2}C devices in slave or master mode
	I2CEXT0_SDA_in		
	I2CEXT1_SCL_in		
	I2CEXT1_SDA_in		
	I2CEXT0_SCL_out		
	I2CEXT0_SDA_out		
	I2CEXT1_SCL_out		
	I2CEXT1_SDA_out		
LED_PWM	ledc_ls_sig_out0~7	Any GPIO pins	8 independent channels, 80 MHz clock/RTC clock/XTAL clock. Duty accuracy: 18 bits.

Interface	Signal	Pin	Function
I^2S	I2S0I_DATA_in0~15	Any GPIO pins	Stereo input and output from/to the audiocodec; parallel LCD data output; parallel camera data input
	I2S0O_BCK_in		
	I2S0O_WS_in		
	I2S0I_BCK_in		
	I2S0I_WS_in		
	I2S0I_H_SYNC		
	I2S0I_V_SYNC		
	I2S0I_H_ENABLE		
	I2S0O_BCK_out		
	I2S0O_WS_out		
	I2S0I_BCK_out		
	I2S0I_WS_out		
	I2S0O_DATA_out0~23		
Infrared Remote controller	RMT_SIG_IN0~3	Any GPIO pins	Four channels for an IR transceiver of various waveforms
	RMT_SIG_OUT0~3		
SPI0/1	SPICLK_out	SPICLK	Support Standard SPI, Dual SPI, QSPI, QPI, OSPI, and OPI. Support STR and DDR modes. Support interface with external flash and RAM.
	SPICS0_out	SPICS0	
	SPICS1_out	SPICS1	
	SPID_in/out	SPID	
	SPIQ_in/out	SPIQ	
	SPIWP_in/out	SPIWP	
	SPIHD_in/out	SPIHD	
	SPID4_in/out	GPIO33	
	SPID5_in/out	GPIO34	
	SPID6_in/out	GPIO35	
	SPID7_in/out	GPIO36	
	SPIDQS_in/out	GPIO37	
SPI2	FSPICLK_in/out	Any GPIO pins	Supports SPI that can interface with LCD and other external devices. Supports the following features: • Both master and slave modes; • Four modes of SPI transfer format; • Configurable SPI frequency; • 72-byte FIFO or DMA buffer. Supports Standard SPI, Dual SPI, QSPI, QPI, OSPI, and OPI. Supports STR and DDR modes. Supports interface with external flash and RAM.
	FSPICS0_in/out		
	FSPICS1 ~ 5_out		
	FSPID_in/out		
	FSPIQ_in/out		
	FSPIWP_in/out		
	FSPIHD_in/out		
	FSPIIO4 ~ 7_in/out		
	FSPIDQS_out		
	FSPICD_out		
	FSPI_VSYNC_out		
	FSPI_HSYNC_out		
	FSPI_DE_out		

Interface	Signal	Pin	Function
SPI3	SPI3_CLK_in/out	Any GPIO pins	Supports Standard SPI, with the following features: • Both master and slave modes; • Four modes of SPI transfer format; • Configurable SPI frequency; • 72-byte FIFO or DMA buffer.
	SPI3_CS0_in/out		
	SPI3_CS1_out		
	SPI3_CS2_out		
	SPI3_D_in/out		
	SPI3_Q_in/out		
	SPI3_HD_in/out		
	SPI3_DQS_out		
	SPI3_CD_out		
Pulse counter	pcnt_sig_ch0_in0	Any GPIO pins	Captures pulse and counts pulse edges in multiple different modes
	pcnt_sig_ch1_in0		
	pcnt_ctrl_ch0_in0		
	pcnt_ctrl_ch1_in0		
	pcnt_sig_ch0_in1		
	pcnt_sig_ch1_in1		
	pcnt_ctrl_ch0_in1		
	pcnt_ctrl_ch1_in1		
	pcnt_sig_ch0_in2		
	pcnt_sig_ch1_in2		
	pcnt_ctrl_ch0_in2		
	pcnt_ctrl_ch1_in2		
	pcnt_sig_ch0_in3		
	pcnt_sig_ch1_in3		
	pcnt_ctrl_ch0_in3		
	pcnt_ctrl_ch1_in3		
USB OTG	D-	GPIO19	Full-speed USB OTG
	D+	GPIO20	

Note:

- GPIO46 is input-only and can not be used for output function.

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 6: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDDA, VDD3P3, VDD3P3_RTC, VDD3P3_CPU, VDD_SPI, VDD3P3_RTC_IO	Voltage applied to power supply pins per power domain	–0.3	3.6	V
T_{STORE}	Storage temperature	–40	150	°C

3.2 Recommended Operating Conditions

Table 7: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDDA, VDD3P3, VDD3P3_RTC	Voltage applied to power supply pins per power domain	2.8	3.3	3.6	V
VDD_SPI (working as input power supply) [1]	—	1.8	3.3	3.6	V
VDD3P3_RTC_IO [2]	—	3.0	3.3	3.6	V
VDD3P3_CPU	Voltage applied to power supply pin	2.8	3.3	3.6	V
I_{VDD}	Current delivered by external power supply	0.5	—	—	A
T_J	Junction temperature	–40	—	125	°C

Note:

1. Please refer to *Power Scheme*, section 1.3, for more information.
2. When VDD_SPI is used to drive peripherals, VDD3P3_RTC_IO should comply with the peripherals' specifications. For more information, please refer to Table 8.
3. When using a single-power supply, the recommended output current is 500 mA or more.

3.3 VDD_SPI Output Characteristics

Table 8: VDD_SPI Output Characteristics

Symbol	Parameter	Typ	Unit
R_{SPI}	On-resistance in 3.3 V mode	5	Ω
I_{SPI}	Output current in 1.8 V mode	40	mA

Note:

In real-life applications, when VDD_SPI works in 3.3 V output mode, VDD3P3_RTC_IO may be affected by R_{SPI}. For example, when VDD3P3_RTC_IO is used to drive an external 3.3 V flash, it should comply with the following specifications:

VDD3P3_RTC_IO > VDD_flash_min + I_flash_max*R_{SPI}

Among which, VDD_flash_min is the minimum operating voltage of the flash, and I_flash_max the maximum current.

For more information, please refer to *Power Scheme*, section 1.3.

3.4 DC Characteristics (3.3 V, 25 °C)

Table 9: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD	—	VDD + 0.3	V
V_{IL}	Low-level input voltage	–0.3	—	0.25 × VDD	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH}	High-level output voltage	0.8 × VDD	—	—	V
V_{OL}	Low-level output voltage	—	—	0.1 × VDD	V
I_{OH}	High-level source current (VDD = 3.3 V, V_{OH} >= 2.64 V, PAD_DRIVER = 3)	—	40	—	mA
I_{OL}	Low-level sink current (VDD = 3.3 V, V_{OL} = 0.495 V, PAD_DRIVER = 3)	—	28	—	mA
R_{PU}	Pull-up resistor	—	45	—	kΩ
R_{PD}	Pull-down resistor	—	45	—	kΩ
V_{IH_nRST}	Chip reset release voltage	0.75 × VDD	—	VDD + 0.3	V
V_{IL_nRST}	Chip reset voltage	–0.3	—	0.25 × VDD	V

Note:
VDD is the I/O voltage for a particular power domain of pins.

3.5 ADC Characteristics

Table 10: ADC Characteristics

Parameter	Description	Min	Max	Unit
DNL (Differential nonlinearity)	RTC controller; ADC connected to an external 100 nF capacitor; DC signal input; ambient temperature at 25 °C; Wi-Fi off	–7	7	LSB
INL (Integral nonlinearity)		–12	12	LSB
Sampling rate	RTC controller	—	200	ksps
	DIG controller	—	2	Msps

Note:

- When reading voltages greater than 2450 mV, ADC accuracy will be worse than that in the table above.
- To get better DNL results, users can sample multiple times and apply a filter, or calculate the average value.

3.6 Current Consumption Characteristics

The current consumption measurements are taken with a 3.3 V supply at 25 °C of ambient temperature at the RF port. All transmitters' measurements are based on a 50% duty cycle.

Table 11: Current Consumption Depending on RF Modes

Work mode	Description		Average	Peak
Active (RF working)	TX	802.11b, 20 MHz, 1 Mbps, @19.5 dBm	190 mA	310 mA
		802.11g, 20 MHz, 54 Mbps, @15 dBm	145 mA	220 mA
		802.11n, 20 MHz, MCS7, @13 dBm	135 mA	200 mA
		802.11n, 40 MHz, MCS7, @13 dBm	120 mA	160 mA
	RX	802.11b/g/n, 20 MHz	63 mA	63 mA
		802.11n, 40 MHz	68 mA	68 mA

Note:

The current consumption figures for in RX mode are for cases when the peripherals are disabled and the CPU idle.

Table 12: Current Consumption Depending on Work Modes

Work mode	Description		Current consumption (Typ)
Modem-sleep	The CPU is powered on	240 MHz	19 mA
		160 MHz	16 mA
		Normal speed: 80 MHz	12 mA
Light-sleep	—		450 μA
Deep-sleep	The ULP co-processor is powered on.		220 μA
	ULP sensor-monitored pattern		7 μA @1% duty
	RTC timer + RTC memory		10 μA
	RTC timer only		5 μA
Power off	CHIP_PU is set to low level, the chip is powered off.		0.1 μA

Note:

- The current consumption figures in Modem-sleep mode are for cases where the CPU is powered on and the cache idle.
- When Wi-Fi is enabled, the chip switches between Active and Modem-sleep modes. Therefore, current consumption changes accordingly.
- In Modem-sleep mode, the CPU frequency changes automatically. The frequency depends on the CPU load and the peripherals used.
- During Deep-sleep, when the ULP co-processor is powered on, peripherals such as GPIO and I^{2}C are able to operate.
- The ”ULP sensor-monitored pattern” refers to the mode where the ULP coprocessor or the sensor works periodically. When touch sensors work with a duty cycle of 1%, the typical current consumption is 7 μA.

3.7 Wi-Fi Radio

3.7.1 Transmitter Characteristics

Table 13: Transmitter Characteristics

Parameter	Rate	Typ	Unit
TX Power	11b, 1 Mbps	19.5	dBm
	11b, 11 Mbps	19.5	
	11g, 6 Mbps	18	
	11g, 54 Mbps	15	
	11n, HT20, MCS0	18	
	11n, HT20, MCS7	13	
	11n, HT40, MCS0	18	
	11n, HT40, MCS7	13	

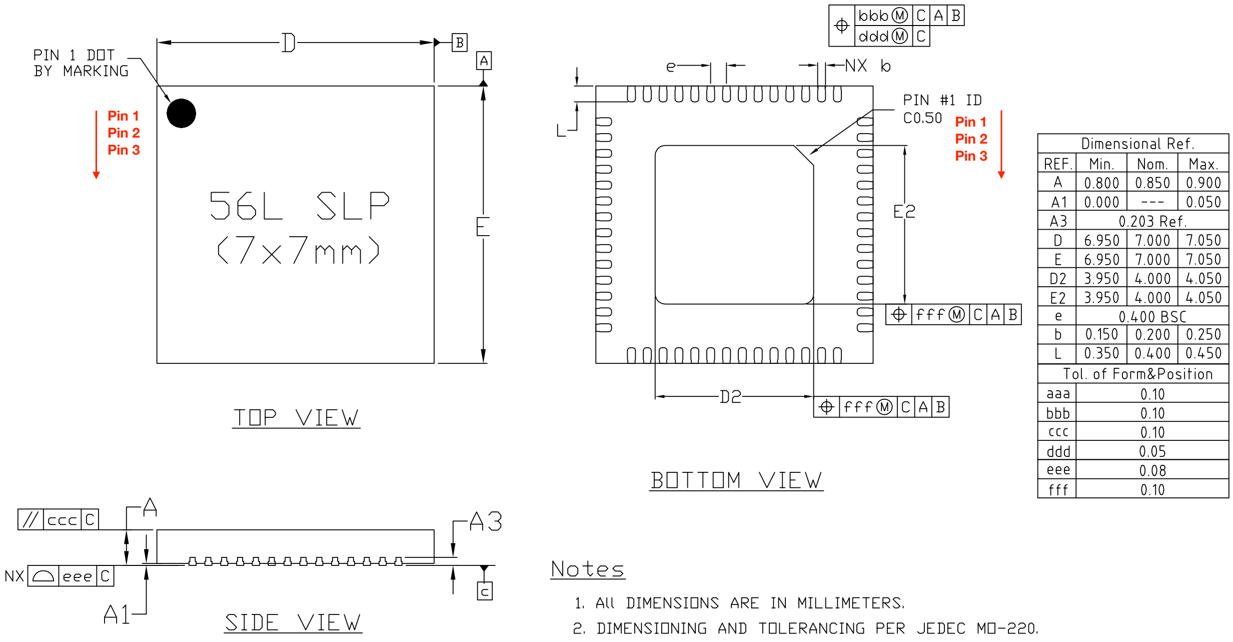
3.7.2 Receiver Characteristics

Table 14: Receiver Characteristics

Parameter	Rate	Typ	Unit
RX Sensitivity	1 Mbps	–97	dBm
	2 Mbps	–95	
	5.5 Mbps	–93	
	11 Mbps	–88	
	6 Mbps	–92	
	9 Mbps	–91	
	12 Mbps	–89	
	18 Mbps	–87	
	24 Mbps	–84	
	36 Mbps	–80	
	48 Mbps	–76	
	54 Mbps	–75	
	11n, HT20, MCS0	–92	
	11n, HT20, MCS1	–88	
	11n, HT20, MCS2	–85	
	11n, HT20, MCS3	–83	
	11n, HT20, MCS4	–79	
	11n, HT20, MCS5	–75	
	11n, HT20, MCS6	–74	
	11n, HT20, MCS7	–72	
	11n, HT40, MCS0	–89	
	11n, HT40, MCS1	–86	
	11n, HT40, MCS2	–83	
	11n, HT40, MCS3	–80	
	11n, HT40, MCS4	–76	

Parameter	Rate	Typ	Unit
	11n, HT40, MCS5	–72	
	11n, HT40, MCS6	–71	
	11n, HT40, MCS7	–69	
RX Maximum Input Level	11b, 1 Mbps	5	dBm
	11b, 11 Mbps	5	
	11g, 6 Mbps	5	
	11g, 54 Mbps	0	
	11n, HT20, MCS0	5	
	11n, HT20, MCS7	0	
	11n, HT40, MCS0	5	
	11n, HT40, MCS7	0	
Adjacent Channel Rejection	11b, 11 Mbps	35	dB
	11g, 6 Mbps	31	
	11g, 54 Mbps	14	
	11n, HT20, MCS0	31	
	11n, HT20, MCS7	13	
	11n, HT40, MCS0	19	
	11n, HT40, MCS7	8	

4. Package Information



Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.800	0.850	0.900
A1	0.000	---	0.050
A3	0.203 Ref.		
D	6.950	7.000	7.050
E	6.950	7.000	7.050
D2	3.950	4.000	4.050
E2	3.950	4.000	4.050
e	0.400 BSC		
b	0.150	0.200	0.250
L	0.350	0.400	0.450
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Notes

1. All DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER JEDEC MO-220.

Figure 6: QFN56 (7×7 mm) Package

Note:
The pins of the chip are numbered in an anti-clockwise direction from Pin 1 in the top view.

Appendix A – ESP32-S2 Pin Lists

A.1. IO MUX

IO_MUX

Pin No.	Power Supply Pin	Analog Pin	Digital Pin	Power Domain	Analog Function0	Analog Function1	RTC_GPIO	Digital Function0	Type	Digital Function1	Type	Digital Function2	Type	Digital Function3	Type	Digital Function4	Type	Drive Strength (Default)	At Reset	After Reset
1	VDDA																			
2	LNA_IN																			
3	VDD3P3																			
4	VDD3P3																			
5			GPIO0	VDD3P3_RTC_IO			RTC_GPIO0	GPIO0	I/O/T	GPIO0	I/O/T							2‘d2	oe=0, ie=1, wpu	oe=0, ie=1, wpu,
6			GPIO1	VDD3P3_RTC_IO	TOUCH1	ADC1_CH0	RTC_GPIO1	GPIO1	I/O/T	GPIO1	I/O/T							2‘d2	oe=0, ie=1	oe=0, ie=1
7			GPIO2	VDD3P3_RTC_IO	TOUCH2	ADC1_CH1	RTC_GPIO2	GPIO2	I/O/T	GPIO2	I/O/T							2‘d2	oe=0, ie=1	oe=0, ie=1
8			GPIO3	VDD3P3_RTC_IO	TOUCH3	ADC1_CH2	RTC_GPIO3	GPIO3	I/O/T	GPIO3	I/O/T							2‘d2	oe=0, ie=1	oe=0, ie=0
9			GPIO4	VDD3P3_RTC_IO	TOUCH4	ADC1_CH3	RTC_GPIO4	GPIO4	I/O/T	GPIO4	I/O/T							2‘d2	oe=0, ie=1	oe=0, ie=0
10			GPIO5	VDD3P3_RTC_IO	TOUCH5	ADC1_CH4	RTC_GPIO5	GPIO5	I/O/T	GPIO5	I/O/T							2‘d2	oe=0, ie=0	oe=0, ie=0
11			GPIO6	VDD3P3_RTC_IO	TOUCH6	ADC1_CH5	RTC_GPIO6	GPIO6	I/O/T	GPIO6	I/O/T							2‘d2	oe=0, ie=0	oe=0, ie=0
12			GPIO7	VDD3P3_RTC_IO	TOUCH7	ADC1_CH6	RTC_GPIO7	GPIO7	I/O/T	GPIO7	I/O/T							2‘d2	oe=0, ie=0	oe=0, ie=0
13			GPIO8	VDD3P3_RTC_IO	TOUCH8	ADC1_CH7	RTC_GPIO8	GPIO8	I/O/T	GPIO8	I/O/T							2‘d2	oe=0, ie=0	oe=0, ie=0
14			GPIO9	VDD3P3_RTC_IO	TOUCH9	ADC1_CH8	RTC_GPIO9	FSPIHD	I1/O/T	GPIO9	I/O/T					FSPIHD	I1/O/T	2‘d2	oe=0, ie=0	oe=0, ie=1
15			GPIO10	VDD3P3_RTC_IO	TOUCH10	ADC1_CH9	RTC_GPIO10	FSPICS0	I1/O/T	GPIO10	I/O/T	FSPIIO4	I1/O/T			FSPICS0	I1/O/T	2‘d2	oe=0, ie=0	oe=0, ie=1
16			GPIO11	VDD3P3_RTC_IO	TOUCH11	ADC2_CH0	RTC_GPIO11	FSPID	I1/O/T	GPIO11	I/O/T	FSPIIO5	I1/O/T			FSPID	I1/O/T	2‘d2	oe=0, ie=0	oe=0, ie=1
17			GPIO12	VDD3P3_RTC_IO	TOUCH12	ADC2_CH1	RTC_GPIO12	FSPICLK	I1/O/T	GPIO12	I/O/T	FSPIIO6	I1/O/T			FSPICLK	I1/O/T	2‘d2	oe=0, ie=0	oe=0, ie=1
18			GPIO13	VDD3P3_RTC_IO	TOUCH13	ADC2_CH2	RTC_GPIO13	FSPIQ	I1/O/T	GPIO13	I/O/T	FSPIIO7	I1/O/T			FSPIQ	I1/O/T	2‘d2	oe=0, ie=0	oe=0, ie=1
19			GPIO14	VDD3P3_RTC_IO	TOUCH14	ADC2_CH3	RTC_GPIO14	FSPIWP	I1/O/T	GPIO14	I/O/T	FSPIDQS	I1/O/T			FSPIWP	I1/O/T	2‘d2	oe=0, ie=0	oe=0, ie=1
20	VDD3P3_RTC																			
21			XTAL_32K_P	VDD3P3_RTC_IO	XTAL_32K_P	ADC2_CH4	RTC_GPIO15	GPIO15	I/O/T	GPIO15	I/O/T	U0RTS	O					2‘d2	oe=0, ie=0	oe=0, ie=0
22			XTAL_32K_N	VDD3P3_RTC_IO	XTAL_32K_N	ADC2_CH5	RTC_GPIO16	GPIO16	I/O/T	GPIO16	I/O/T	U0CTS	I1					2‘d2	oe=0, ie=0	oe=0, ie=0
23			DAC_1	VDD3P3_RTC_IO	DAC_1	ADC2_CH6	RTC_GPIO17	GPIO17	I/O/T	GPIO17	I/O/T	U1TXD	O					2‘d2	oe=0, ie=0	oe=0, ie=1
24			DAC_2	VDD3P3_RTC_IO	DAC_2	ADC2_CH7	RTC_GPIO18	GPIO18	I/O/T	GPIO18	I/O/T	U1RXD	I1	CLK_OUT3	O			2‘d2	oe=0, ie=0	oe=0, ie=1
25			GPIO19	VDD3P3_RTC_IO	USB_D-	ADC2_CH8	RTC_GPIO19	GPIO19	I/O/T	GPIO19	I/O/T	U1RTS	O	CLK_OUT2	O			2‘d2	oe=0, ie=0	oe=0, ie=0
26			GPIO20	VDD3P3_RTC_IO	USB_D+	ADC2_CH9	RTC_GPIO20	GPIO20	I/O/T	GPIO20	I/O/T	U1CTS	I1	CLK_OUT1	O			2‘d2	oe=0, ie=0	oe=0, ie=0
27	VDD3P3_RTC_IO																			
28			GPIO21	VDD3P3_RTC_IO			RTC_GPIO21	GPIO21	I/O/T	GPIO21	I/O/T							2‘d2	oe=0, ie=0	oe=0, ie=0
29			SPICS1	VDD_SPI				SPICS1	I1/O/T	GPIO26	I/O/T							2‘d2	oe=0, ie=1, wpu	oe=1, ie=1, wpu
30	VDD_SPI																			
31			SPIHD	VDD_SPI				SPIHD	I1/O/T	GPIO27	I/O/T							2‘d2	oe=0, ie=1, wpu	oe=0, ie=1, wpu
32			SPIWP	VDD_SPI				SPIWP	I1/O/T	GPIO28	I/O/T							2‘d2	oe=0, ie=1, wpu	oe=0, ie=1, wpu
33			SPICS0	VDD_SPI				SPICS0	I1/O/T	GPIO29	I/O/T							2‘d2	oe=0, ie=1, wpu	oe=1, ie=1, wpu
34			SPICLK	VDD_SPI				SPICLK	I1/O/T	GPIO30	I/O/T							2‘d2	oe=0, ie=1, wpu	oe=1, ie=1, wpu
35			SPIQ	VDD_SPI				SPIQ	I1/O/T	GPIO31	I/O/T							2‘d2	oe=0, ie=1, wpu	oe=0, ie=1, wpu
36			SPID	VDD_SPI				SPID	I1/O/T	GPIO32	I/O/T							2‘d2	oe=0, ie=1, wpu	oe=0, ie=1, wpu
37			GPIO33	VDD3P3_CPU / VDD_SPI				GPIO33	I/O/T	GPIO33	I/O/T	FSPIHD	I1/O/T			SPIIO4	I1/O/T	2‘d2	oe=0, ie=0	oe=0, ie=1
38			GPIO34	VDD3P3_CPU / VDD_SPI				GPIO34	I/O/T	GPIO34	I/O/T	FSPICS0	I1/O/T			SPIIO5	I1/O/T	2‘d2	oe=0, ie=0	oe=0, ie=1
39			GPIO35	VDD3P3_CPU / VDD_SPI				GPIO35	I/O/T	GPIO35	I/O/T	FSPID	I1/O/T			SPIIO6	I1/O/T	2‘d2	oe=0, ie=0	oe=0, ie=1
40			GPIO36	VDD3P3_CPU / VDD_SPI				GPIO36	I/O/T	GPIO36	I/O/T	FSPICLK	I1/O/T			SPIIO7	I1/O/T	2‘d2	oe=0, ie=0	oe=0, ie=1
41			GPIO37	VDD3P3_CPU / VDD_SPI				GPIO37	I/O/T	GPIO37	I/O/T	FSPIQ	I1/O/T			SPIDQS	I1/O/T	2‘d2	oe=0, ie=0	oe=0, ie=1
42			GPIO38	VDD3P3_CPU				GPIO38	I/O/T	GPIO38	I/O/T	FSPIWP	I1/O/T			GPIO38	I/O/T	2‘d2	oe=0, ie=0	oe=0, ie=1
43			MTCK	VDD3P3_CPU				MTCK	I1	GPIO39	I/O/T	CLK_OUT3	O					2‘d2	oe=0, ie=0	oe=0, ie=1
44			MTDO	VDD3P3_CPU				MTDO	O/T	GPIO40	I/O/T	CLK_OUT2	O					2‘d2	oe=0, ie=0	oe=0, ie=1
45	VDD3P3_CPU																			
46			MTDI	VDD3P3_CPU				MTDI	I1	GPIO41	I/O/T	CLK_OUT1	O					2‘d2	oe=0, ie=0	oe=0, ie=1
47			MTMS	VDD3P3_CPU				MTMS	I0	GPIO42	I/O/T							2‘d2	oe=0, ie=0	oe=0, ie=1
48			U0TXD	VDD3P3_CPU				U0TXD	O	GPIO43	I/O/T	CLK_OUT1	O					2‘d2	oe=0, ie=1, wpu	oe=1, ie=1, wpu
49			U0RXD	VDD3P3_CPU				U0RXD	I1	GPIO44	I/O/T	CLK_OUT2	O					2‘d2	oe=0, ie=1, wpu	oe=0, ie=1, wpu
50			GPIO45	VDD3P3_CPU				GPIO45	I/O/T	GPIO45	I/O/T							2‘d2	oe=0, ie=1, wpd	oe=0, ie=1, wpd
51	VDDA																			
52		XTAL_N																		
53		XTAL_P																		
54	VDDA																			
55			GPIO46	VDD3P3_CPU				GPIO46	I	GPIO46	I								oe=0, wpd, ie=1	oe=0, wpd, ie=1
56		CHIP_PU		VDD3P3_RTC_IO																
Total	10	3	43																	

Notes:

- Power supply for GPIO33, GPIO34, GPIO35, GPIO36 and GPIO37 is configurable to be either VDD3P3_CPU (default) or VDD_SPI.
- wpu: weak pull-up
- wpd: weak pull-down
- ie: input enable
- oe: output enable
- Each column about digital “Function" is accompanied by a column about “Type". Please see the following explanations for the meanings of “type" with respect to each “function" they are associated with. For each “Function-*N*", “type" signifies:
  - I: input only. If a function other than “Function-*N*" is assigned, the input signal of “Function-*N*" is still from this pin.
  - I1: input only. If a function other than “Function-*N*" is assigned, the input signal of “Function-*N*" is always “1".
  - I0: input only. If a function other than “Function-*N*" is assigned, the input signal of “Function-*N*" is always “0".
  - O: output only.
  - T: high-impedance.
  - I/O/T: combinations of input, output, and high-impedance according to the function signal.
  - I1/O/T: combinations of input, output, and high-impedance, according to the function signal. If a function is not selected, the input signal of the function is “1”.

A.2. GPIO Matrix

Table 15: GPIO Matrix

Signal No.	Input signals	Default value if unassigned *	Same input signal from IO MUX core	Output signals	Output enable of output signals
0	SPIQ_in	0	yes	SPIQ_out	SPIQ_oe
1	SPID_in	0	yes	SPID_out	SPID_oe
2	SPIHD_in	0	yes	SPIHD_out	SPIHD_oe
3	SPIWP_in	0	yes	SPIWP_out	SPIWP_oe
4	-	-	-	SPICLK_out_mux	SPICLK_oe
5	-	-	-	SPICS0_out	SPICS0_oe
6	-	-	-	SPICS1_out	SPICS1_oe
7	SPID4_in	0	yes	SPID4_out	SPID4_oe
8	SPID5_in	0	yes	SPID5_out	SPID5_oe
9	SPID6_in	0	yes	SPID6_out	SPID6_oe
10	SPID7_in	0	yes	SPID7_out	SPID7_oe
11	SPIDQS_in	0	yes	SPIDQS_out	SPIDQS_oe
14	U0RXD_in	0	yes	U0TXD_out	1’d1
15	U0CTS_in	0	yes	U0RTS_out	1’d1
16	U0DSR_in	0	no	U0DTR_out	1’d1
17	U1RXD_in	0	yes	U1TXD_out	1’d1
18	U1CTS_in	0	yes	U1RTS_out	1’d1
21	U1DSR_in	0	no	U1DTR_out	1’d1
23	I2S0O_BCK_in	0	no	I2S0O_BCK_out	1’d1
25	I2S0O_WS_in	0	no	I2S0O_WS_out	1’d1
27	I2S0I_BCK_in	0	no	I2S0I_BCK_out	1’d1
28	I2S0I_WS_in	0	no	I2S0I_WS_out	1’d1
29	I2CEXT0_SCL_in	1	no	I2CEXT0_SCL_out	I2CEXT0_SCL_oe
30	I2CEXT0_SDA_in	1	no	I2CEXT0_SDA_out	I2CEXT0_SDA_oe
39	pcnt_sig_ch0_in0	0	no	gpio_wlan_prio	1’d1
40	pcnt_sig_ch1_in0	0	no	gpio_wlan_active	1’d1
41	pcnt_ctrl_ch0_in0	0	no	-	1’d1
42	pcnt_ctrl_ch1_in0	0	no	-	1’d1
43	pcnt_sig_ch0_in1	0	no	-	1’d1
44	pcnt_sig_ch1_in1	0	no	-	1’d1
45	pcnt_ctrl_ch0_in1	0	no	-	1’d1
46	pcnt_ctrl_ch1_in1	0	no	-	1’d1
47	pcnt_sig_ch0_in2	0	no	-	1’d1
48	pcnt_sig_ch1_in2	0	no	-	1’d1
49	pcnt_ctrl_ch0_in2	0	no	-	1’d1
50	pcnt_ctrl_ch1_in2	0	no	-	1’d1
51	pcnt_sig_ch0_in3	0	no	-	1’d1
52	pcnt_sig_ch1_in3	0	no	-	1’d1

Signal No.	Input signals	Default value if unassigned *	Same input signal from IO MUX core	Output signals	Output enable of output signals
53	pcnt_ctrl_ch0_in3	0	no	-	1'd1
54	pcnt_ctrl_ch1_in3	0	no	-	1'd1
64	usb_otg_iddig_in	0	no	-	1'd1
65	usb_otg_avalid_in	0	no	-	1'd1
66	usb_srp_bvalid_in	0	no	usb_otg_idpullup	1'd1
67	usb_otg_vbusvalid_in	0	no	usb_otg_dppulldown	1'd1
68	usb_srp_sessend_in	0	no	usb_otg_dmpulldown	1'd1
69	-	-	-	usb_otg_drvvbus	1'd1
70	-	-	-	usb_srp_chrgvbus	1'd1
71	-	-	-	usb_srp_dischrgvbus	1'd1
72	SPI3_CLK_in	0	no	SPI3_CLK_out_mux	SPI3_CLK_oe
73	SPI3_Q_in	0	no	SPI3_Q_out	SPI3_Q_oe
74	SPI3_D_in	0	no	SPI3_D_out	SPI3_D_oe
75	SPI3_HD_in	0	no	SPI3_HD_out	SPI3_HD_oe
76	SPI3_CS0_in	0	no	SPI3_CS0_out	SPI3_CS0_oe
77	-	-	-	SPI3_CS1_out	SPI3_CS1_oe
78	-	-	-	SPI3_CS2_out	SPI3_CS2_oe
79	-	-	-	ledc_ls_sig_out0	1'd1
80	-	-	-	ledc_ls_sig_out1	1'd1
81	-	-	-	ledc_ls_sig_out2	1'd1
82	-	-	-	ledc_ls_sig_out3	1'd1
83	rmt_sig_in0	0	no	ledc_ls_sig_out4	1'd1
84	rmt_sig_in1	0	no	ledc_ls_sig_out5	1'd1
85	rmt_sig_in2	0	no	ledc_ls_sig_out6	1'd1
86	rmt_sig_in3	0	no	ledc_ls_sig_out7	1'd1
87	-	-	-	rmt_sig_out0	1'd1
88	-	-	-	rmt_sig_out1	1'd1
89	-	-	-	rmt_sig_out2	1'd1
90	-	-	-	rmt_sig_out3	1'd1
95	I2CEXT1_SCL_in	1	no	I2CEXT1_SCL_out	I2CEXT1_SCL_oe
96	I2CEXT1_SDA_in	1	no	I2CEXT1_SDA_out	I2CEXT1_SDA_oe
100	-	-	-	gpio_sd0_out	1'd1
101	-	-	-	gpio_sd1_out	1'd1
102	-	-	-	gpio_sd2_out	1'd1
103	-	-	-	gpio_sd3_out	1'd1
104	-	-	-	gpio_sd4_out	1'd1
105	-	-	-	gpio_sd5_out	1'd1
106	-	-	-	gpio_sd6_out	1'd1
107	-	-	-	gpio_sd7_out	1'd1
108	FSPICLK_in	0	yes	FSPICLK_out_mux	FSPICLK_oe
109	FSPIQ_in	0	yes	FSPIQ_out	FSPIQ_oe

Signal No.	Input signals	Default value if unassigned *	Same input signal from IO MUX core	Output signals	Output enable of output signals
110	FSPID_in	0	yes	FSPID_out	FSPID_oe
111	FSPIHD_in	0	yes	FSPIHD_out	FSPIHD_oe
112	FSPIWP_in	0	yes	FSPIWP_out	FSPIWP_oe
113	FSPIIO4_in	0	yes	FSPIIO4_out	FSPIIO4_oe
114	FSPIIO5_in	0	yes	FSPIIO5_out	FSPIIO5_oe
115	FSPIIO6_in	0	yes	FSPIIO6_out	FSPIIO6_oe
116	FSPIIO7_in	0	yes	FSPIIO7_out	FSPIIO7_oe
117	FSPICS0_in	0	yes	FSPICS0_out	FSPICS0_oe
118	-	-	-	FSPICS1_out	FSPICS1_oe
119	-	-	-	FSPICS2_out	FSPICS2_oe
120	-	-	-	FSPICS3_out	FSPICS3_oe
121	-	-	-	FSPICS4_out	FSPICS4_oe
122	-	-	-	FSPICS5_out	FSPICS5_oe
123	can_rx	1	no	can_tx	1’d1
124	-	-	-	can_bus_off_on	1’d1
125	-	-	-	can_clkout	1’d1
126	-	-	-	SUBSPICLK_out_mux	SUBSPICLK_oe
127	SUBSPIQ_in	0	yes	SUBSPIQ_out	SUBSPIQ_oe
128	SUBSPID_in	0	yes	SUBSPID_out	SUBSPID_oe
129	SUBSPIHD_in	0	yes	SUBSPIHD_out	SUBSPIHD_oe
130	SUBSPIWP_in	0	yes	SUBSPIWP_out	SUBSPIWP_oe
131	-	-	-	SUBSPICS0_out	SUBSPICS0_oe
132	-	-	-	SUBSPICS1_out	SUBSPICS1_oe
133	-	-	-	FSPIDQS_out	FSPIDQS_oe
134	-	-	-	FSPI_HSYNC_out	FSPI_HSYNC_oe
135	-	-	-	FSPI_VSYNC_out	FSPI_VSYNC_oe
136	-	-	-	FSPI_DE_out	FSPI_DE_oe
137	-	-	-	FSPICD_out	FSPICD_oe
139	-	-	-	SPI3_CD_out	SPI3_CD_oe
140	-	-	-	SPI3_DQS_out	SPI3_DQS_oe
143	I2S0I_DATA_in0	0	no	I2S0O_DATA_out0	1’d1
144	I2S0I_DATA_in1	0	no	I2S0O_DATA_out1	1’d1
145	I2S0I_DATA_in2	0	no	I2S0O_DATA_out2	1’d1
146	I2S0I_DATA_in3	0	no	I2S0O_DATA_out3	1’d1
147	I2S0I_DATA_in4	0	no	I2S0O_DATA_out4	1’d1
148	I2S0I_DATA_in5	0	no	I2S0O_DATA_out5	1’d1
149	I2S0I_DATA_in6	0	no	I2S0O_DATA_out6	1’d1
150	I2S0I_DATA_in7	0	no	I2S0O_DATA_out7	1’d1
151	I2S0I_DATA_in8	0	no	I2S0O_DATA_out8	1’d1
152	I2S0I_DATA_in9	0	no	I2S0O_DATA_out9	1’d1
153	I2S0I_DATA_in10	0	no	I2S0O_DATA_out10	1’d1

Signal No.	Input signals	Default value if unassigned *	Same input signal from IO MUX core	Output signals	Output enable of output signals
154	I2S0I_DATA_in11	0	no	I2S0O_DATA_out11	1'd1
155	I2S0I_DATA_in12	0	no	I2S0O_DATA_out12	1'd1
156	I2S0I_DATA_in13	0	no	I2S0O_DATA_out13	1'd1
157	I2S0I_DATA_in14	0	no	I2S0O_DATA_out14	1'd1
158	I2S0I_DATA_in15	0	no	I2S0O_DATA_out15	1'd1
159	-	-	-	I2S0O_DATA_out16	1'd1
160	-	-	-	I2S0O_DATA_out17	1'd1
161	-	-	-	I2S0O_DATA_out18	1'd1
162	-	-	-	I2S0O_DATA_out19	1'd1
163	-	-	-	I2S0O_DATA_out20	1'd1
164	-	-	-	I2S0O_DATA_out21	1'd1
165	-	-	-	I2S0O_DATA_out22	1'd1
166	-	-	-	I2S0O_DATA_out23	1'd1
167	SUBSPID4_in	0	yes	SUBSPID4_out	SUBSPID4_oe
168	SUBSPID5_in	0	yes	SUBSPID5_out	SUBSPID5_oe
169	SUBSPID6_in	0	yes	SUBSPID6_out	SUBSPID6_oe
170	SUBSPID7_in	0	yes	SUBSPID7_out	SUBSPID7_oe
171	SUBSPIDQS_in	0	yes	SUBSPIDQS_out	SUBSPIDQS_oe
193	I2S0I_H_SYNC	0	no	-	1'd1
194	I2S0I_V_SYNC	0	no	-	1'd1
195	I2S0I_H_ENABLE	0	no	-	1'd1
215	-	-	-	ant_sel0	1'd1
216	-	-	-	ant_sel1	1'd1
217	-	-	-	ant_sel2	1'd1
218	-	-	-	ant_sel3	1'd1
219	-	-	-	ant_sel4	1'd1
220	-	-	-	ant_sel5	1'd1
221	-	-	-	ant_sel6	1'd1
222	-	-	-	ant_sel7	1'd1
223	sig_in_func_223	0	no	sig_in_func223	1'd1
224	sig_in_func_224	0	no	sig_in_func224	1'd1
225	sig_in_func_225	0	no	sig_in_func225	1'd1
226	sig_in_func_226	0	no	sig_in_func226	1'd1
227	sig_in_func_227	0	no	sig_in_func227	1'd1
235	pro_alonegpio_in0	0	no	pro_alonegpio_out0	1'd1
236	pro_alonegpio_in1	0	no	pro_alonegpio_out1	1'd1
237	pro_alonegpio_in2	0	no	pro_alonegpio_out2	1'd1
238	pro_alonegpio_in3	0	no	pro_alonegpio_out3	1'd1
239	pro_alonegpio_in4	0	no	pro_alonegpio_out4	1'd1
240	pro_alonegpio_in5	0	no	pro_alonegpio_out5	1'd1
241	pro_alonegpio_in6	0	no	pro_alonegpio_out6	1'd1

Signal No.	Input signals	Default value if unassigned *	Same input signal from IO MUX core	Output signals	Output enable of output signals
242	pro_alonegpio_in7	0	no	pro_alonegpio_out7	1'd1
251	-	-	-	clk_i2s_mux	1'd1

Revision History

Date	Version	Release notes
2019.11	V0.4	Updated Section 2.6.2: *Ultra-Low-Power Co-processor*; Updated Section 2.7: *Timers and Watchdogs*; Updated Table 15: *GPIO Matrix*; Added documentation feedback hyperlink; Fixed formatting issues; Other small changes.
2019.08	V0.3	Overall update.
2019.06	V0.2	Updated Figure 3: *ESP32-S2 Power Scheme*; Updated Section 1.4: *Strapping Pins*; Updated Figure 5: *Address Mapping Structure*; Updated Section 3: *Electrical Characteristics.*
2019.04	V0.1	Preliminary release.