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# N720 Mini PCIe Hardware User Guide

## (AUDIO)

## Version 1.0

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## Notice

This document provides guide for users to use the N720 Mini PCIe (AUDIO).

This document is intended for system engineers (SEs), development engineers, and test engineers.

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| Revision Record | | |
|---|---|---|
| **Version** | **Changes** | **Date** |
| V1.0 | Initial draft | 2017-07 |



# Contents

# Table of Figures

# Table of Tables

# 1 Overview

N720 is an industrial-grade 4G module developed on Qualcomm platform. This module has an ultra-wide operating temperature range of -40 ℃ to +85 ℃ and electrostatic capacity of 8 kV. N720 Mini PCIe complies with the PCI Express Mini Card 1.2 standard and provides various application interfaces in addition to standard interfaces. It is well applicable to video surveillance, notebook, in-vehicle devices, wireless routers, and other IoT terminals with the following features:

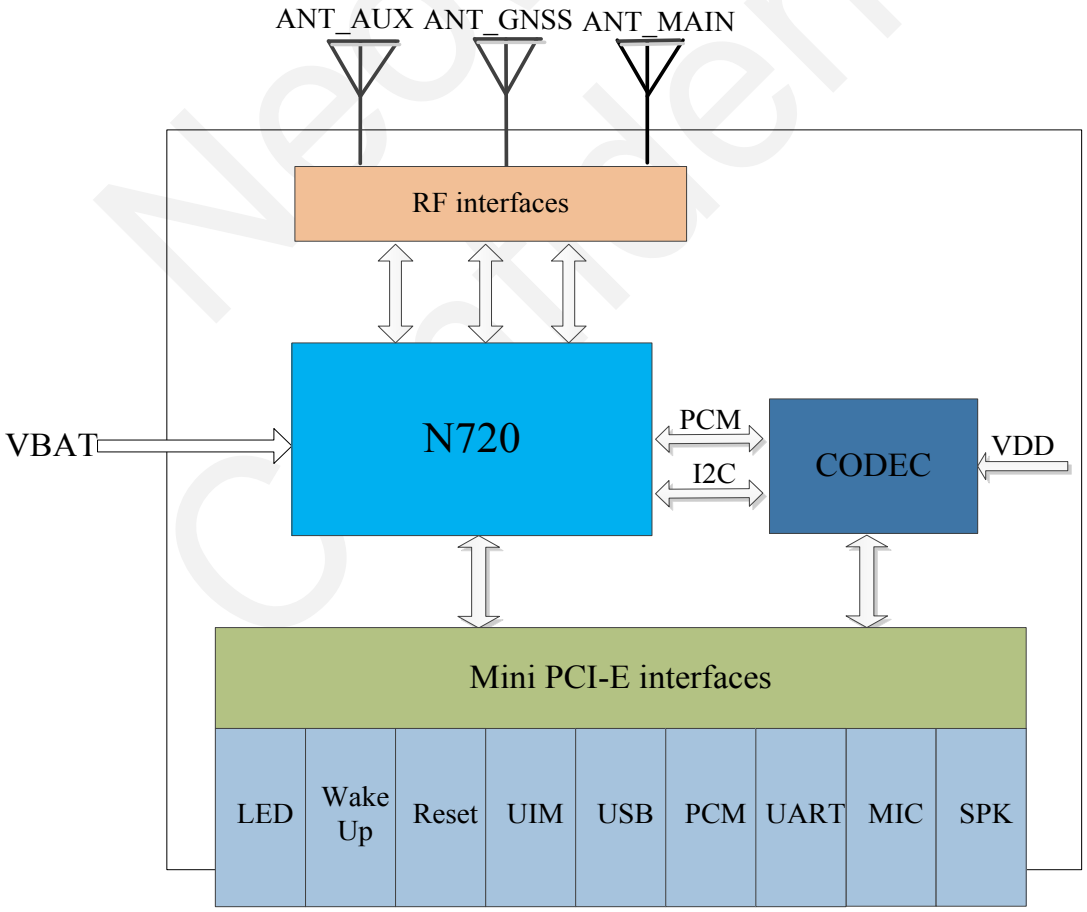
- ARM Cortex-A7 processor, 1.3 GHz main frequency, 256 KB L2 cache, 28 nm process technology
- GSM/GPRS/EDGE & CDMA2000 1x/1xAdvanced/1xEV-DOrA &&WCDMA R99 to DC-HSPA+&&TD-SCDMA&LTE Cat4
- USB2.0/ UIM/ UART/PCM/GNSS/AUDIO

This document describes the block diagram, features, pin description, reference design for application interfaces, mounting packaging, and storage.

## 1.1 Block Diagram

Figure 1-1 shows the block diagram of N720.

**Figure 1-1** N720 Mini PCIe block diagram



## 1.2 Bands

Mounted N720 modules with different configurations, N720 Mini PCIe series include the following versions to meet the band requirements in different areas:

| Module | Version | Area | Category | Band |
|---|---|---|---|---|
| N720 Mini PCIe | CA | China | Cat4 | FDD-LTE: B1, B3, B5, B8<br>TDD-LTE: B38, B39, B40, B41<br>TD-SCDMA: B34, B39<br>UMTS: B1, B8<br>EV-DO: BC0<br>CDMA 1x: BC0<br>GSM/GPRS/EDGE: 900/1800 MHz |
| | CB | China | Cat4 | FDD-LTE: B1, B3, B5, B8<br>TDD-LTE: B38, B39, B40, B41<br>TD-SCDMA: B34, B39<br>UMTS: B1, B8<br>GSM/GPRS/EDGE: 900/1800 MHz |
| | CC | China | Cat4 | FDD-LTE: B1, B3, B8, B28<br>TDD-LTE: B38, B39, B40, B41<br>TD-SCDMA: B34, B39<br>UMTS: B1, B8<br>GSM/GPRS/EDGE: 900/1800 MHz |
| | EA | Europe | Cat4 | FDD-LTE: B1, B3, B5, B7, B8, B20<br>TDD-LTE: B40<br>UMTS: B1, B8<br>GSM/GPRS/EDGE: 850/900/1800/1900 MHz |
| | UA | the United States | Cat4 | FDD-LTE: B2, B4, B5, B7, B12, B17<br>UMTS: B2, B4, B5<br>GSM/GPRS/EDGE: 850/900/1800/1900 MHz |
| | JA | Japan | Cat4 | FDD-LTE: B1, B3, B8, B9, B19<br>UMTS: B1, B8, B9, B19 |
| | IA | India | Cat4 | FDD-LTE: B3, B5<br>TDD-LTE: B40<br>UMTS: B1, B8<br>GSM/GPRS/EDGE: 850/900/1800/1900 MHz |

# 2 Features

**Table 2-1** N720 Mini PCIe baseband and wireless features

| Specifications | Description |
|---|---|
| Power supply | 3.0V to 3.6V; Typical value: 3.3 V |
| Current in sleep mode | <4 mA |
| Idle current | <25 mA |
| Operating temperature | -40 °C to +85 °C |
| Processor | ARM Cortex-A7 processor<br>Main frequency: 1.3 GHz<br>256 kB L2 cache |
| Memory | RAM: 256 MB<br>ROM: 256 MB |
| Band | See Table 2-1. |
| Rate | GPRS: Max 85.6 Kbps(DL) / Max 85.6 Kbps(U)<br>CDMA: Max 3.1 Mbps (DL) / Max 1.8 Mbps (UL)<br>WCDMA: DC-HSPA+, Max 42 Mbps(DL)/Max 5.76 Mbps(UL)<br>TD-SCDMA: Max 4.2 Mbps(DL)/Max 2.2 Mbps(UL)<br>FDD-LTE: non-CA cat4, Max 150 Mbps(DL)/Max 50 Mbps(UL)<br>TDD-LTE: non-CA cat4, Max 130 Mbps(DL)/Max 35 Mbps(UL) |
| Transmit power | GSM850: +33 dBm (Power Class 4)<br>EGSM900: +33 dBm (Power Class 4)<br>DCS1800: +30 dBm (Power Class 1)<br>PCS1900: +30 dBm (Power Class 1)<br>EDGE 850 MHz: +27 dBm (Power Class E2)<br>EDGE 900 MHz: +27 dBm (Power Class E2)<br>EDGE 1800 MHz: +26 dBm (Power Class E2)<br>EDGE 1900 MHz: +26 dBm (Power Class E2)<br>TD-SCDMA:+23 dBm (Power Class 3)<br>CDMA 1X/EVDO:+23 dBm(Power Class 3)<br>UMTS: 23 dBm (Power Class 3)<br>LTE: +23 dBm (Power Class 3) |
| Antenna feature | 2G/3G/4G main antenna, 4G diversity antenna, GNSS antenna, 50 Ω impedance |
| UART | At most 4 Mbps, 1 groups |
| UIM | 1 group of UIM, 1.8V/3V dual-voltage adaptive |
| USB | 1 group of USB2.0 high-speed interface |
| PCM | 1 group of PCM interface |

| | |
|---|---|
| AUDIO | MIC/ SPK differential analog audio interface<br>The I/O volume is adjustable. |

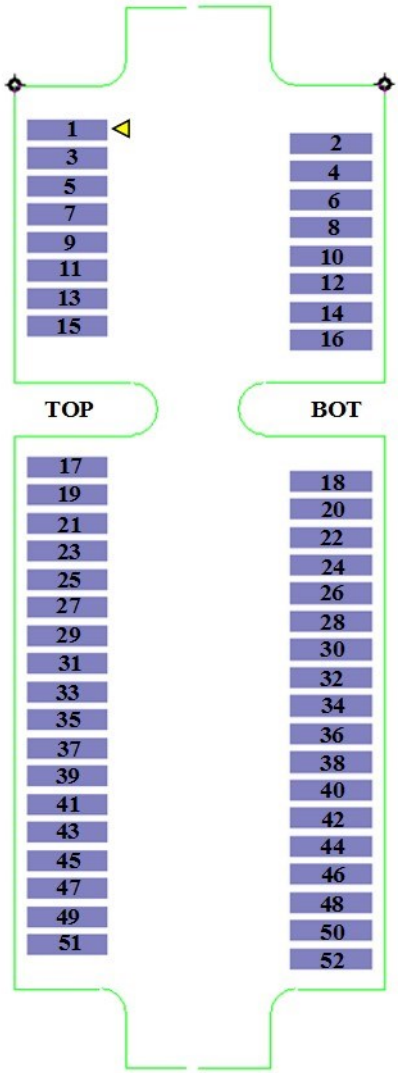
# 3 Application Interfaces

## 3.1 Pin Description

N720 Mini PCIe has 52 pins, including general function pins and other pins. Figure 3-1 defines the pins.

**Figure 3-1** N720 Mini PCIe pin description

| Pin Name | No. |
|---|---|
| MIC_P | 1 |
| MIC_N | 3 |
| SPK_P | 5 |
| SPK_N | 7 |
| GND | 9 |
| VREG_1V8 | 11 |
| NC | 13 |
| GND | 15 |
| NC | 17 |
| WAKEUP_IN | 19 |
| GND | 21 |
| UART_RX | 23 |
| UART_RTS | 25 |
| GND | 27 |
| GND | 29 |
| UART_TX | 31 |
| PON_RESET | 33 |
| GND | 35 |
| GND | 37 |
| V_MAIN | 39 |
| V_MAIN | 41 |
| GND | 43 |
| PCM_CLK | 45 |
| PCM_DIN | 47 |
| PCM_OUT | 49 |
| PCM_SYNC | 51 |




| No. | Pin Name |
|---|---|
| 2 | V_MAIN |
| 4 | GND |
| 6 | NC |
| 8 | V_USIM |
| 10 | USIM_DATA |
| 12 | USIM_CLK |
| 14 | USIM_RST |
| 16 | NC |
| 18 | GND |
| 20 | W_DISABLE |
| 22 | PON_RESET |
| 24 | V_MAIN |
| 26 | GND |
| 28 | UART_CTS |
| 30 | UART_DCD |
| 32 | WAKEUP_OUT |
| 34 | GND |
| 36 | USB_D- |
| 38 | USB_D+ |
| 40 | GND |
| 42 | LED_WWAN |
| 44 | USIM_DETECT |
| 46 | UART_DTR |
| 48 | NC |
| 50 | GND |
| 52 | V_MAIN |

NOTE

IO: input/output
DO: Digital output
PO: Power output
AO: Analog output
DI: Digital input
PI: Power input
AI: Analog input
OC: Open collector

**Table 3-1** N720 Mini PCIe pin description

| Name | Pin | I/O | Function | Level Feature (V) | Power Domain | Remarks |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| V_MAIN | 2, 24, 39, 41, 52 | PI | Main power supply | Vmin=3.0 V<br>Vmax=3.6 V<br>Vtyp=3.3 V | | Maximum supply current of 3 A peak. |
| VREG_1P8 | 11 | PO | 1.8 V power supply | Vnorm=1.8 V;<br>Imax=50 mA; | 1.8 V | Supply power for IO level shifting circuit.<br>Leave this pin unconnected if it is not used. |
| GND | 4, 9, 15, 18 21, 26, 27, 29, 34, 35, 37, 40, 43, 50 | | GND | | | |
| PON RESET | 22, 33 | DI | Reset input | | | Low level triggers the reset. |
| **UART** | | | | | | |
| UART_TX | 31 | DO | UART data transmit | $V_{OL}$ max=0.45 V;<br>$V_{OH}$ min=1.35 V; | 1.8 V | Data transmission<br>Leave these pins unconnected if they are not used. |
| UART_RX | 23 | DI | UART data receive | $V_{IL}$ min=-0.3 V;<br>$V_{IL}$ max=0.45 V;<br>$V_{IH}$ min=1.35 V;<br>$V_{IH}$ max=2.1 V | 1.8 V | |

| | | | | | | |
|---|---|---|---|---|---|---|
| UART_CTS | 28 | DI | Clear to send | $V_{IL}$ min=-0.3 V;<br>$V_{IL}$ max=0.45 V;<br>$V_{IH}$ min=1.35 V;<br>$V_{IH}$ max=2.1 V | 1.8 V | Leave these pins unconnected if they are not used. |
| UART_RTS | 25 | DO | Request to send | $V_{OL}$ max=0.45 V;<br>$V_{OH}$ min=1.35 V | 1.8 V | |
| UART_DTR | 46 | DI | Data terminal is ready | $V_{IL}$ min=-0.3V;<br>$V_{IL}$ max=0.45V;<br>$V_{IH}$ min=1.35V;<br>$V_{IH}$ max=2.1V | 1.8V | Leave this pin unconnected if it is not used. |
| UART_DCD | 30 | DO | Data carrier detect | $V_{OL}$ max=0.45V;<br>$V_{OH}$ min=1.35V | 1.8V | Leave this pin unconnected if it is not used. |
| **UIM** | | | | | | |
| V_USIM | 8 | PO | UIM power supply output | 1.8V USIM:<br>Vmax = 1.9 V ;<br>Vmin = 1.7 V<br>3V USIM:<br>Vmax = 3.05 V;<br>Vmin = 2.7 V;<br>IO max =50 mA | 1.8 V/3 V | Compatible with 1.8/3V UIM card |
| USIM_RST | 14 | DO | UIM reset | 1.8 V USIM:<br>$V_{OL}$ max = 0.45 V;<br>$V_{OH}$ min = 1.35 V<br>3 V USIM:<br>$V_{OL}$ max = 0.4 V;<br>$V_{OH}$ min = 2.6V | 1.8 V/3 V | |

| | | | | | | |
|---|---|---|---|---|---|---|
| USIM_DATA | 10 | IO | UIM data input/output | 1.8V USIM:<br>$V_{IL}$ max = 0.6 V;<br>$V_{IH}$ min = 1.2 V;<br>$V_{OL}$ max = 0.45 V;<br>$V_{OH}$ min = 1.35 V<br>3V USIM:<br>$V_{IL}$ max = 0.8 V<br>$V_{IH}$ min = 1.95 V<br>$V_{OL}$ max = 0.45 V<br>$V_{OH}$ min = 2.6 V | 1.8 V/3 V | |
| USIM_CLK | 12 | DO | UIM clock output | 1.8 V USIM:<br>$V_{OL}$ max = 0.45 V;<br>$V_{OH}$ min = 1.35 V<br>3V USIM:<br>$V_{OL}$ max = 0.4 V<br>$V_{OH}$ min = 2.6 V | 1.8 V/3 V | |
| USIM_DETECT | 44 | DI | UIM detect | $V_{IL}$ min = -0.3 V;<br>$V_{IL}$ max = 0.63 V | 1.8 V | |
| **USB** | | | | | | |
| USB_D- | 36 | IO | Negative signal of USB data | USB2.0 | | Used for program download and data transmission.<br>Differential traces<br>90 Ω impedance |
| USB_D+ | 38 | IO | positive signal of USB data | USB2.0 | | |
| **PCM** | | | | | | |
| PCM_CLK | 45 | IO | PCM clock signal | VOL max=0.45V;<br>VOH min=1.35V | 1.8V | Leave these pins unconnected if they are not used. |

| | | | | | | |
|---|---|---|---|---|---|---|
| PCM_DIN | 47 | DI | PCM data input | VIL min=-0.3V;<br>VIL max=0.45V;<br>VIH min=1.6V;<br>VIH max=2.1V | 1.8V | |
| PCM_DOUT | 49 | DO | PCM data output | VOL max=0.45V;<br>VOH min=1.35V | 1.8V | |
| PCM_SYNC | 51 | IO | PCM synchronize signal | VOL max=0.45V;<br>VOH min=1.35V;<br>VIL min=-0.3V;<br>VIL max=0.45V;<br>VIH min=1.6V;<br>VIH max=2.1V | 1.8V | |
| Audio | | | | | | |
| MIC_P | 1 | AI | Positive of audio input | Differential input | 1.8 V | Leave them unconnected if it is not used. |
| MIC_N | 3 | AI | Negative of audio input | | | |
| SPK_P | 5 | AO | Positive of audio output | Differential output | | Leave them unconnected if it is not used. |
| SPK_N | 7 | AO | Negative of audio output | | | |
| **Other Pins** | | | | | | |
| LED_WWAN | 42 | OC | Network status indicator | | | Leave this pin unconnected if it is not used. |
| WAKEUP_IN | 19 | DI | Sleep mode control | $V_{IL}$ min=-0.3V;<br>$V_{IL}$ max=0.45V;<br>$V_{IH}$ min=1.35V;<br>$V_{IH}$ max=2.1V | 1.8V | Leave this pin unconnected if it is not used. |

| | | | | | | |
|---|---|---|---|---|---|---|
| WAKEUP_OUT | 32 | DO | Sleep mode status indicator | $V_{OL}$ max=0.45V;<br>$V_{OH}$ min=1.35V | 1.8V | Leave this pin unconnected if it is not used. |
| W_DISABLE | 20 | DI | Disable RF communication | $V_{IL}$ min=-0.3V;<br>$V_{IL}$ max=0.45V;<br>$V_{IH}$ min=1.35V;<br>$V_{IH}$ max=2.1V | 1.8V | Leave this pin unconnected if it is not used. |
| NC | 6, 13, 16, 17, 48 | | NC | | | Leave them unconnected.<br>Do not use them. |

# 3.2 Application Interfaces

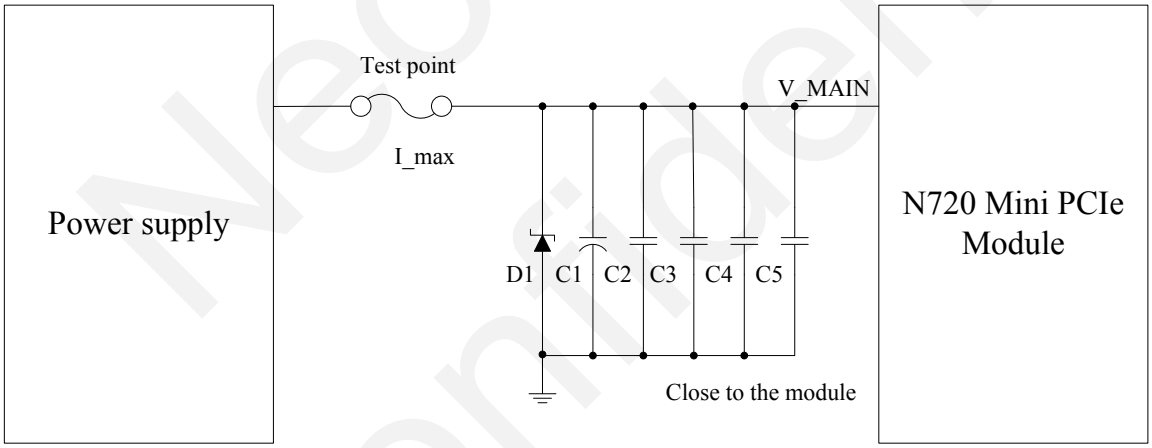
This section introduces the reference design for main application interfaces.

## 3.2.1 V_MAIN

| Name | Pin | I/O | Function | Remarks |
|---|---|---|---|---|
| V_MAIN | 2, 24, 39, 41, 52 | PI | Main power supply input | 3.0 V to 3.6 V (typical value: 3.3 V) |

V_MAIN is the power supply input pin of the N720 Mini PCIe module. Its input voltage ranges from 3.0 V to 3.6 V and the typical value is 3.3 V. In addition to baseband, it supplies power to RF power amplifier and audio circuit. The performance of the V_MAIN power supply is a critical path to module's performance and stability. The input current at the V_MAIN pin will reach its peak of 3A when the signal is weak and the module works at the maximum transmitting power. The voltage will encounter a drop in such a situation. The module might restart if the voltage drops lower than 3.0 V.
The reference design of the V_MAIN power supply is shown as below:

**Figure 3-2** Capacitors used for the power supply




In Figure 3-2, use TVS at D1 to enhance the performance of the module during a burst. SMF5.0AG (Vrwm=5 V&Pppm=200 W) is recommended. A large bypass tantalum capacitor (220 µF or 100 µF) or aluminum capacitor (470 µF or 1000 µF) is expected at C1 to reduce voltage drops during bursts together with C2 (10 µF ceramics capacitor).In addition, add 0.1 µF, 100 pF, and 33 pF filter capacitors to enhance the stability of the power supply.

## 3.2.2 VREG_1V8

| Name | Pin | I/O | Function | Remarks |
|---|---|---|---|---|
| VREG_1V8 | 11 | PO | 1.8 V power supply | Supply power for IO level shifting circuit. Leave this pin unconnected if it is not used. |

VREG_1V8 outputs 1.8 V voltage. It is recommended that VREG_1.8 V@50 mA be used only for interface level.

### 3.2.3 PON_RESET

The PON_RESET pin is used to reset the module by hardware. Low level for more than 1 second at this pin triggers module reset. Figure 3-3 shows the reference design. If 1.8 V IO system is used to control the module reset, connect to this pin directly.

**Figure 3-3** Reference design of hardware reset

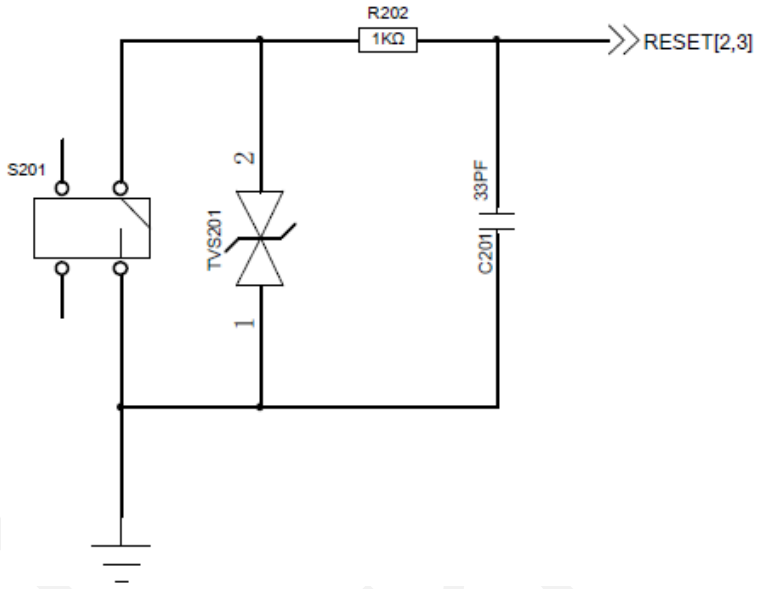



**Figure 3-4** Reset control by external IO

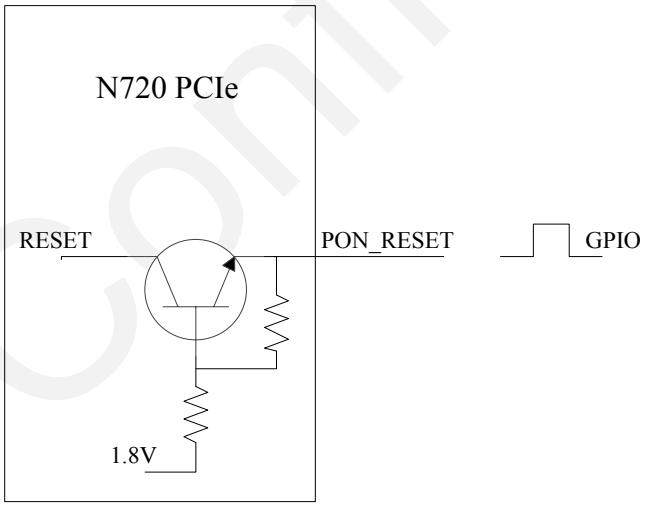
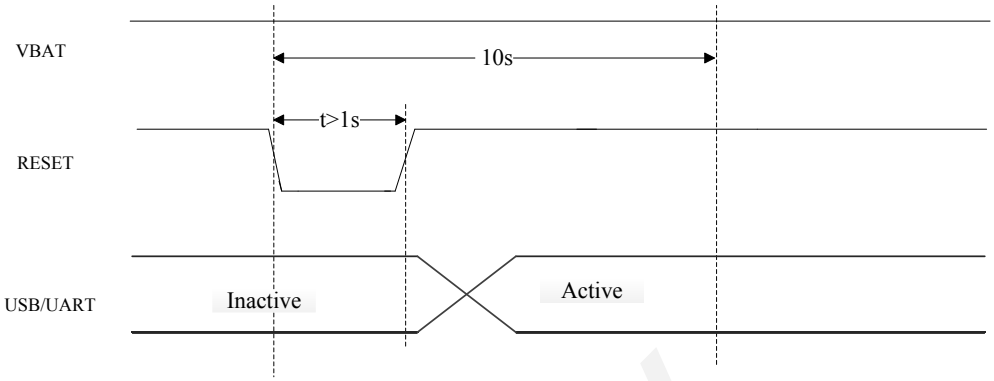



Figure 3-5 shows the reset sequence.

**Figure 3-5** N720 PCIe reset sequence

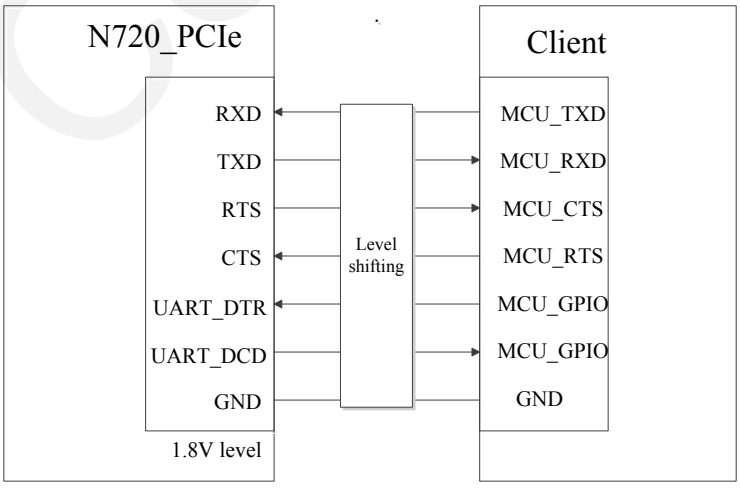



## 3.2.4 UART

| Name | Pin | I/O | Function | Remarks |
|---|---|---|---|---|
| UART_TX | 31 | DO | UART data transmit | Data transmission |
| UART_RX | 23 | DI | UART data receive | Data transmission |
| UART_CTS | 28 | DI | Clear to send | Leave this pin unconnected if it is not used. |
| UART_RTS | 25 | DO | Request to send | Leave this pin unconnected if it is not used. |
| UART_DTR | 46 | DI | Data terminal ready | Leave this pin unconnected if it is not used. |
| UART_DCD | 30 | DO | Data carrier detect | Leave this pin unconnected if it is not used. |

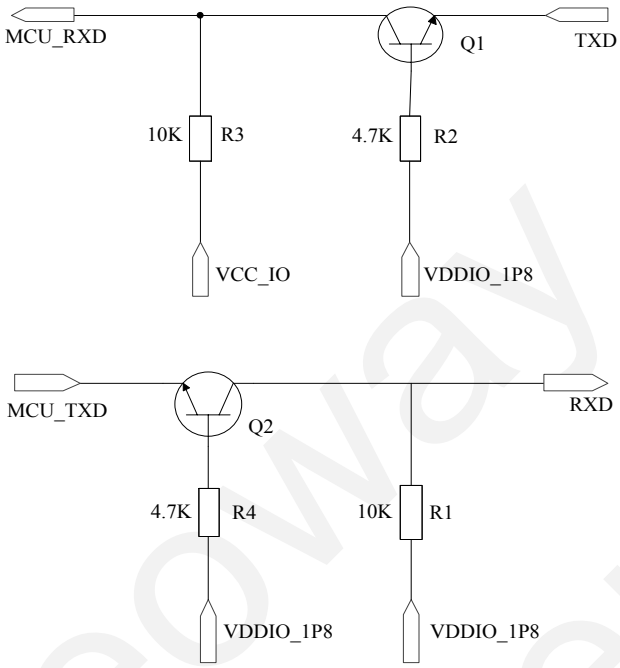
N720 PCIe provides 1 group of UART interface, which supports hardware flow control and at the rate of 4 Mbps at most. The level at the interface is 1.8V. Figure 3-6 shows the reference design of the UART interface.

**Figure 3-6** UART connection



If the UART does not match the logic voltage of the MCU, add a level shifting circuit outside of the module as shown in Figure 3-7 (for $V_{OL}$≤200 mV) and Figure 3-8 (for $V_{OL}$>200 mV).

**Figure 3-7** Recommended level shifting circuit 1

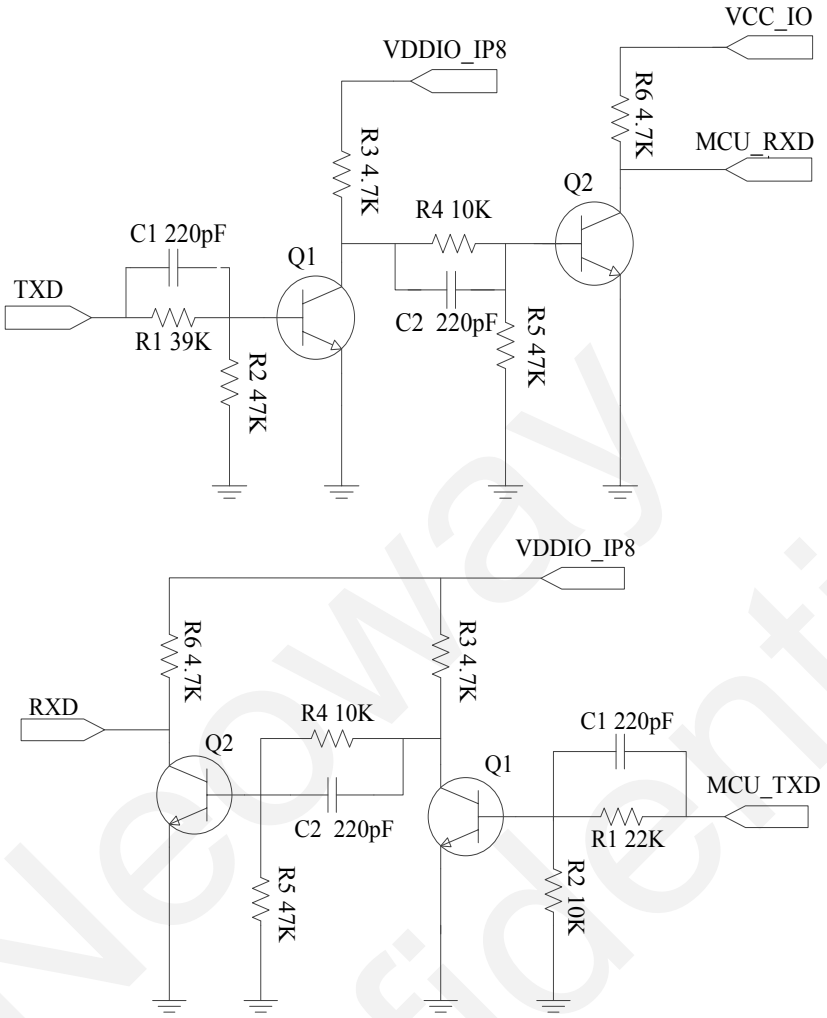



NOTE

Components:
R2/R4: 2K-10K. The greater the UART baud rate is, the lower the R2/R4 values are.
R1/R3: 4.7K-10K The greater the UART baud rate is, the lower the R/R3R3 value is.
Q1/Q2: MMBT3904 or MMBT2222. High-speed transistor is better.

MCU_TXD and MCU_RXD are respectively the TX and RX ports of the MCU while TXD and RXD are respectively the TX and RX ports of the module.
Voltage at VCC_IO is the voltage at the UART of the MCU while voltage at VDDIO_1V8 is the voltage at the UART of the module.
Figure 3-8 shows another recommended level shifting circuit.

**Figure 3-8** Recommended level shifting circuit 2




NOTE

Components: Q1/Q2: MMBT3904 or MMBT2222. High-speed transistors are better.

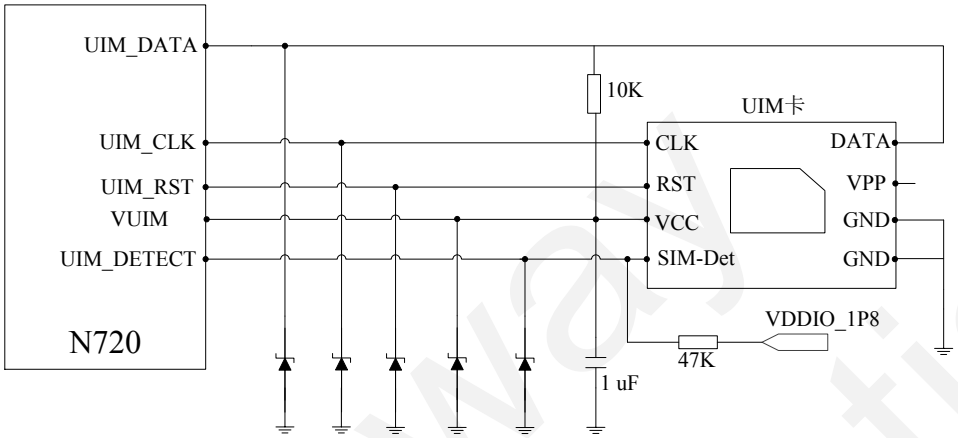
MCU_TXD and MCU_RXD are respectively the TX and RX ports of the MCU, while TXD and RXD are respectively the TX and RX ports of the module.
Voltage at VCC_IO is the voltage at the UART of the MCU while voltage at VDDIO_1V8 is the voltage at the UART of the module.

## 3.2.5 USIM

| Name | Pin | I/O | Function | Remarks |
|---|---|---|---|---|
| V_USIM | 8 | PO | 1.8V/3.3V | UIM power supply output |
| USIM_RST | 14 | DO | 1.8V/3.3V | UIM reset |
| USIM_DATA | 10 | IO | 1.8V/3.3V | UIM data input/output |
| USIM _CLK | 12 | DO | 1.8V/3.3V | UIM clock |
| USIM_DETECT | 44 | DI | 1.8V | UIM detect |

N720 PCIe supports 1.8V/3V UIM cards. V_USIM is the power supply pin of the UIM card and its maximum load is 30 mA. The USIM_DATA pin is pulled up by 10 kΩ resistor internally, so an external pull-up resistor is not necessary in design. USIM_CLK is the clock signal pin, supporting 3.25 GHz of clock frequency. Figure 3-9 shows the reference design of the UIM card interface.

**Figure 3-9** Reference design of SIM card interface




ESD protectors, such as ESD diodes or ESD varistors (with a junction capacitance of less than 33 pF), are recommended to be added on the SIM signals, especially in automotive or other applications with bad ESD. Replace the ESD diodes with 27 pF to 33 pF capacitors connecting to GND in common applications. The ESD diodes or small capacitors should be close to UIM card.
N720 PCIe supports SIM card detection. UIM_DETECT is a 1.8 V interrupt pin. Low level means UIM card detected while high level means no UIM card detected.

**CAUTION**

The antenna should be installed far away from the UIM card and UIM card traces, especially to the built-in antenna.
The UIM traces on the PCB should be as short as possible and shielded with GND copper.
The ESD protection diodes or small capacitors should be close to UIM card on the PCB.

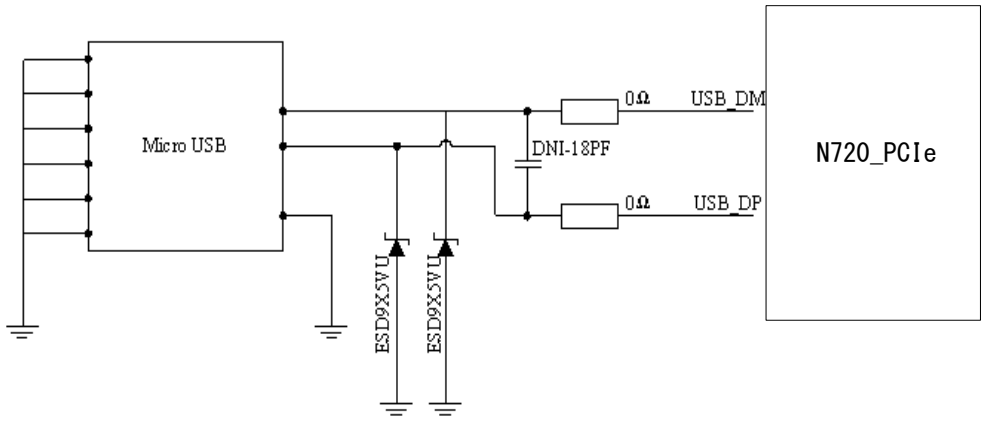
## 3.2.6 USB

| Name | Pin | I/O | Function | Remarks |
|---|---|---|---|---|
| USB_D- | 36 | IO | negative signal of USB data | Used for firmware download and data transmission<br>Differential trace<br>90Ω impedance |
| USB_D+ | 38 | IO | positive signal of USB data | |

USB can be used for firmware download, data communication, and commissioning. Figure 3-10 shows the recommended USB circuit.

**Figure 3-10** Recommended resign of USB circuit




The junction capacitance of the TVS protection diodes for USB_D+ and USB_D- should be lower than 12 pF as possible. USB data lines adopt differential trace design, in which the differential impedance is limited to 90 Ω characteristic impedance. Isolate the traces from other signal traces.

## 3.2.7 PCM

| Name | Pin | I/O | Function | Level | Remarks |
|---|---|---|---|---|---|
| PCM_CLK | 45 | IO | PCM clock signal | 1.8V | Leave these pins unconnected if they are not used. |
| PCM_DIN | 47 | DI | PCM data input | 1.8V | |
| PCM_DOUT | 49 | DO | PCM data output | 1.8V | |
| PCM_SYNC | 51 | IO | PCM synchronize | 1.8V | |

N720 PCIe provides one PCM interface that supports host and client device mode. The reference level at the interface is 1.8 V.

The following figures shows the PCM sequence and connection.

**Figure 3-11** PCM sequence

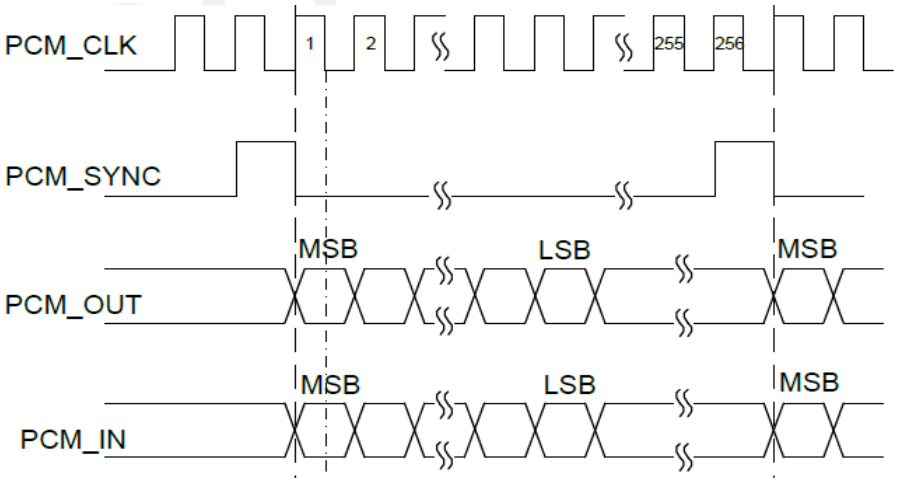
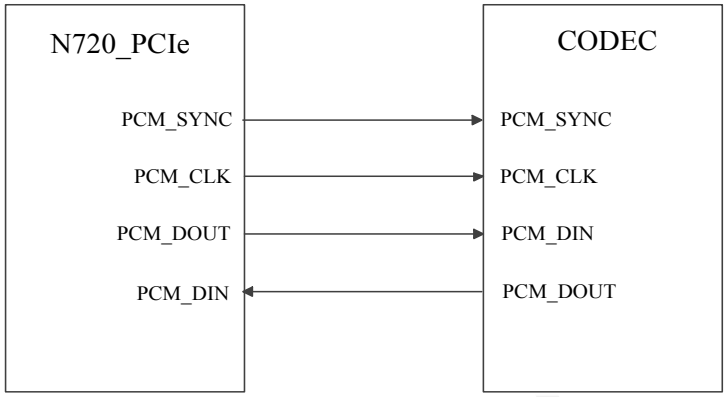


**Figure 3-12** PCM connection




## 3.2.8 Analog Audio

| Name | Pin | I/O | Function | Level Feature | Remarks |
|---|---|---|---|---|---|
| MIC_P | 1 | AI | Negative of audio output | Differential input | Leave these pins unconnected if they are not used. |
| MIC_N | 3 | AI | Positive of audio output | | |
| SPK_P | 5 | AO | Positive of audio output | differential input | Leave these pins unconnected if they are not used. |
| SPK_P | 7 | AO | Negative of audio output | | |

MIC_P and MIC_N are used for differential MIC input. Electret MIC is recommended.
SPK_P and SPK_N are used for differential speaker or receiver output. An audio amplifier is required.
On the PCB board, bead, filter capacitor, and ESD components should be as closer to the audio components or pins as possible. The trace should be far away from interference sources and as shorter as possible. The differential traces should comply with the design rules.
The volume of MIC and SPK can be adjusted via API commands. For details, see *Neoway_N720_Command_Mannual*.
No bias circuit is required externally because there is a bias voltage for the electret MIC in the module.

**Figure 3-13** Reference MIC design

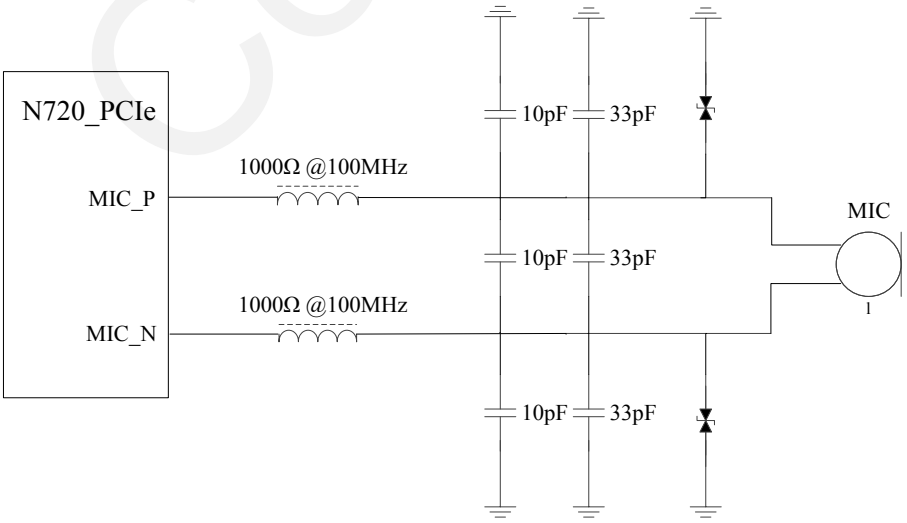


**Figure 3-14** Reference receiver design

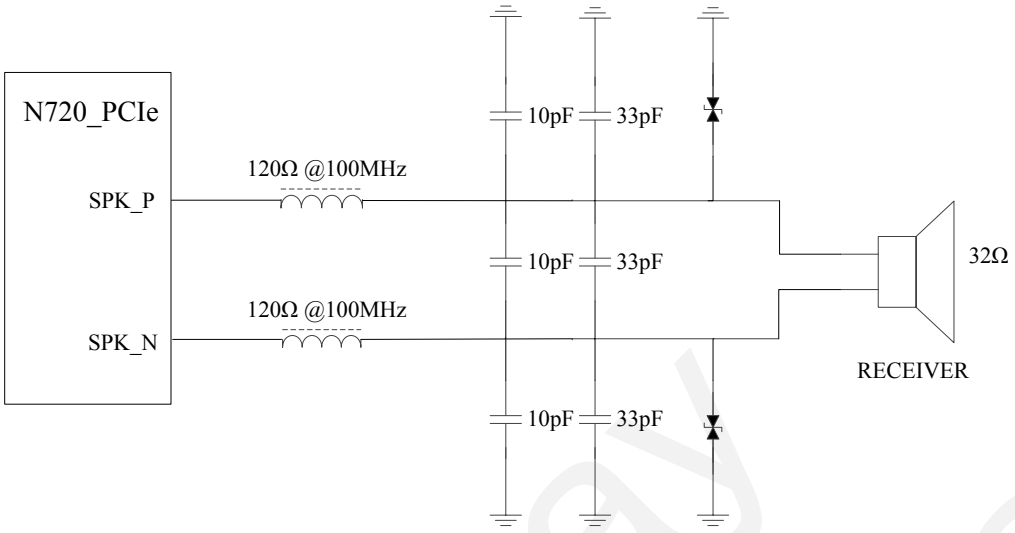
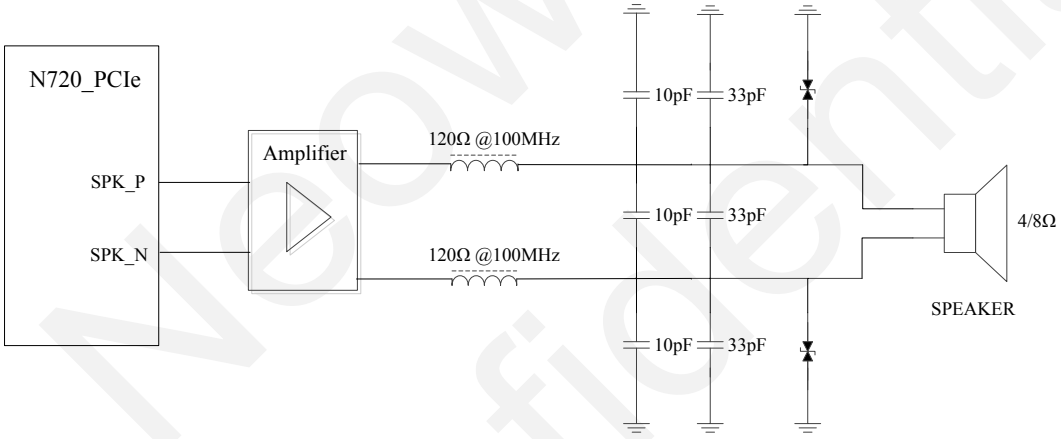



**Figure 3-15** Reference speaker design



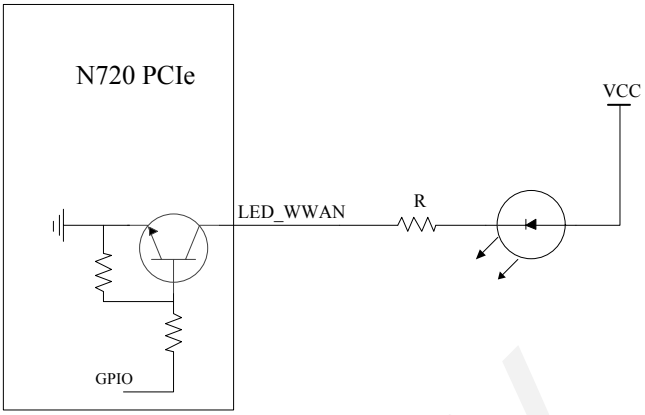

## 3.2.9 Other Interfaces

| Name | Pin | I/O | Function | Level Feature | Remarks |
|---|---|---|---|---|---|
| LED_WWAN | 42 | OC | Network status indicator | | OC |
| WAKEUP_IN | 19 | DI | Sleep mode control | 1.8V | |
| WAKEUP_OUT | 32 | DO | Sleep mode indicator | 1.8V | |
| W_DISABLE | 20 | DI | Disable RF communication | 1.8V | |

### LED_WWAN

The LED_WWAN interface uses an OC output and the maximum input current reaches 20 mA. Connect a resistor in series when connecting an LED. The resistance can be adjusted according to the brightness of the LED. The LED is glowed when low level is at the LED_WWAN pin.

**Figure 3-16** LED_WWAN reference design




## WAKEUP_IN and WAKEUP_OUT

The WAKEUP_IN pin is used to control sleep mode together with AT commands. Enable the sleep mode function by AT command. Then pulling WAKEUP_IN low will bring the module into sleep mode if the module is idle. In this mode, the idle current is less than 4 mA, depending on the DRX setting of network. In sleep mode, the module can respond to the incoming call, SMS, and data. The host MCU can also control the module to exit sleep mode by controlling WAKEUP_IN.

Process of entering sleep mode:

1. Keep WAKEUP_IN high level in normal working mode. Activate the sleep mode by using the **AT+ENPWRSAVE=1** command.
2. Pull WAKEUP_IN low, and the module will enter sleep mode, but only after process and pending data finished.
3. In sleep mode, the external MCP can pull WAKEUP_IN high so that the module will exit from sleep mode actively. Then the module can transmit data and initiate calls. After processing is finished, pull WAKEUP_IN low again to take the module back to sleep mode.
4. In sleep mode, the module can be woken up by the events of incoming voice call, received data, or SMS. Meanwhile the module will send out the unsolicited messages through the UART.

   Upon receipt of the unsolicited messages, the host MCU should pull WAKEUP_IN high firstly, otherwise the module will resume sleep mode in two minutes after the service processing. Then the host MCU can process the voice call, received data, or SMS. After processing is finished, pull WAKEUP_IN low again to put the module into sleep mode.

The WAKEUP_OUT pin is used to indicate whether the module is in sleep mode.

## W_DISABLE

The W_DISABLE pin is used to disable the RF communication of the module. It works with software support.

# 4 Antenna Interfaces

## 4.1 Interface Types

N720_PCIe module provides three interfaces respectively for 2G/3G/4G main antenna, 4G diversity antenna, and GNSS antenna. Figure 4-1 shows their positions on the PCIe module.

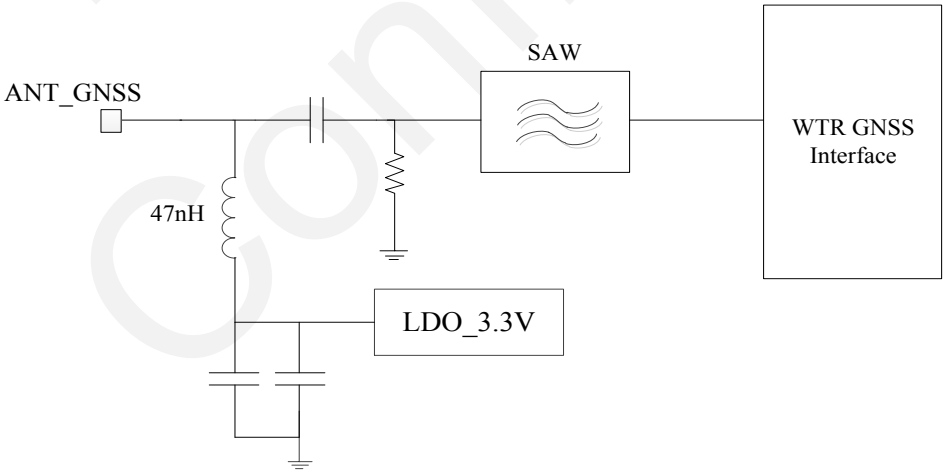
**Figure 4-1** N720_PCIe antenna interfaces


Antennas connecting to the module must comply with mobile device standards: a VSWR ranging from 1.1 to 1.5 and 50 Ω impedance. The antennas should be well matched to achieve the best performance. They should be installed far away from high-speed logic circuits, DC/DC power or any other strong disturbing sources.

## 4.2 GNSS Antenna

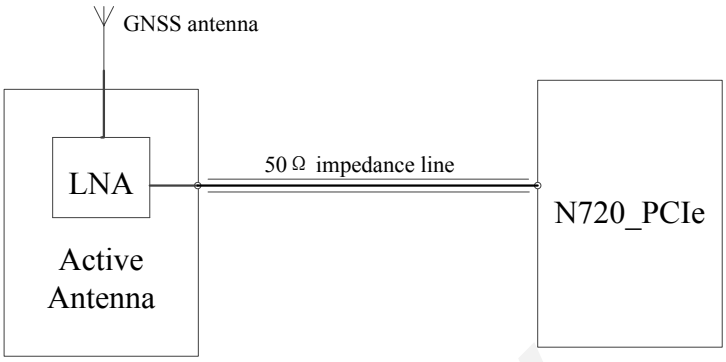
Figure 4-2 shows the circuit of GNSS RF inside the N720 Mini PCIe module.

**Figure 4-2** Internal GNSS RF circuit




If the GNSS signal is poor, the electric signal converted will be very poor and easy to get interference. So, an active antenna is recommended. The poor signal that the active GNSS antenna receives will be amplified by an LNA and then transmitted to the internal IC through the feeder. The N720 Mini PCIe module supplies 3.3 V power for the active antenna internally and connects to it through a 47 nH inductor. The GNSS antenna can be an active ceramic antenna.

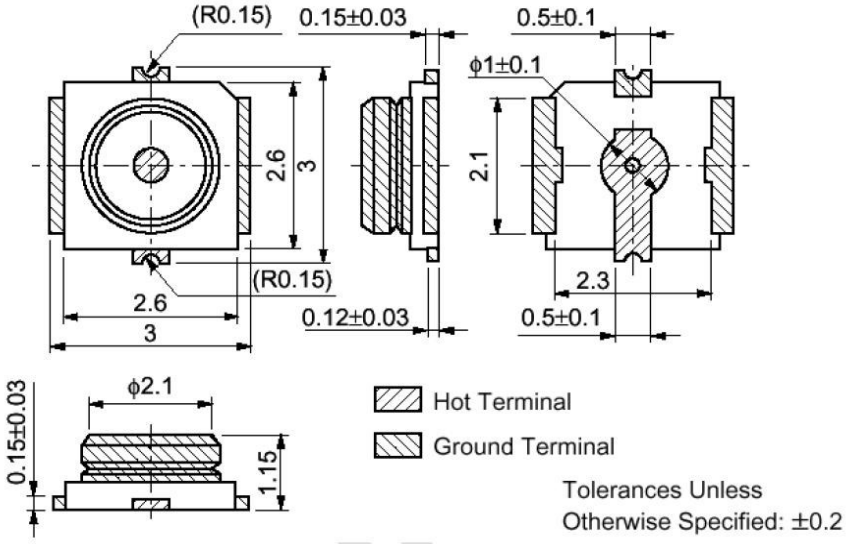
**Figure 4-3** Active antenna connection




# 4.3 RF Connector

To adopt RF antenna connections, the GSC RF connector MM9329-2700RA1 from Murata is recommended. Figure 4-4 shows the encapsulation specifications.

**Figure 4-4** Encapsulation specifications of Murata RF connector



# 5 Electrical Features and Reliability

## 5.1 Temperature

**Table 5-1** Temperature feature

| Module Status | Minimum Value | Typical Value | Maximum Value |
|---|---|---|---|
| Work | -40 °C | 25 °C | 85 °C |
| Storage | -45 °C | | 90 °C |

**CAUTION**

If the module works in temperature exceeding the thresholds, some of its RF performance indicators might be worse but it can still work properly.

## 5.2 Working Band

**Table 5-2** N720 Mini PCIe working band

| Working Band | Uplink | Downlink |
|---|---|---|
| GSM850 | 824~849 MHz | 869~894 MHz |
| EGSM900 | 880~915 MHz | 925~960 MHz |
| DCS1800 | 1710~1785 MHz | 1805~1880 MHz |
| PCS1900 | 1850~1910 MHz | 1930~1990 MHz |
| CDMA BC0 | 824~849 MHz | 869~894 MHz |
| UMTS B1 | 1920~1980 MHz | 2110~2170 MHz |
| UMTS B2 | 1850~1910 MHz | 1930~1990 MHz |
| UMTS B4 | 1710~1755 MHz | 2110~2155 MHz |
| UMTS B5 | 824~849 MHz | 869~894 MHz |
| UMTS B8 | 880~915 MHz | 925~960 MHz |
| UMTS B9 | 1749.9~1784.9 MHz | 1844.9~1879.9 MHz |
| UMTS B19 | 869~894 MHz | 869~894 MHz |
| TD-SCDMA B34 | 2010~2025 MHz | 2010~2025 MHz |
| TD-SCDMA B39 | 1880~1920 MHz | 1880~1920 MHz |
| FDD-LTE B1 | 1920~1980 MHz | 2110~2170 MHz |
| FDD-LTE B2 | 1850~1910 MHz | 1930~1990 MHz |
| FDD-LTE B3 | 1710~1785 MHz | 1805~1880 MHz |

| | | |
|---|---|---|
| FDD-LTE B4 | 1710~1755 MHz | 2110~2155 MHz |
| FDD-LTE B5 | 824~849 MHz | 869~894 MHz |
| FDD-LTE B7 | 2500~2570 MHz | 2620~2690 MHz |
| FDD-LTE B8 | 880~915MHz | 925~960 MHz |
| FDD-LTE B9 | 1749.9~1784.9MHz | 1844.9~1879.9 MHz |
| FDD-LTE B12 | 699~716 MHz | 728~746 MHz |
| FDD-LTE B17 | 704~716 MHz | 734~746 MHz |
| FDD-LTE B19 | 830~845 MHz | 875~890 MHz |
| FDD-LTE B20 | 832~862 MHz | 791~821 MHz |
| FDD-LTE B28 | 703~748 MHz | 758~803 MHz |
| TDD-LTE B38 | 2570~2620 MHz | 2570~2620 MHz |
| TDD-LTE B39 | 1880~1920 MHz | 1880~1920 MHz |
| TDD-LTE B40 | 2300~2400 MHz | 2300~2400 MHz |
| TDD-LTE B41 | 2555~2655 MHz | 2555~2655 MHz |

## 5.3 TX Power and RX Sensitivity

**Table 5-3** N720 Mini PCIe RF power and RX sensitivity

| Band | Transmitting Power | Receiving Sensitivity |
|---|---|---|
| GSM850 | 33dBm+2/-2 dBm | <-108 dBm |
| EGSM900 | 33dBm+2/-2 dBm | <-108 dBm |
| DCS1800 | 30dBm+2/-2 dBm | <-108 dBm |
| PCS1900 | 30dBm+2/-2 dBm | <-108 dBm |
| CDMA BC0 | 24dBm +1/-1 dBm | <-107 dBm |
| UMTS B1 | 24dBm +1/-3 dBm | <-108 dBm |
| UMTS B2 | 24dBm +1/-3 dBm | <-108 dBm |
| UMTS B4 | 24dBm +1/-3 dBm | <-108 dBm |
| UMTS B5 | 24dBm +1/-3 dBm | <-108 dBm |
| UMTS B8 | 24dBm +1/-3 dBm | <-108 dBm |
| UMTS B9 | 24dBm +1/-3 dBm | <-108 dBm |
| UMTS B19 | 24dBm +1/-3 dBm | <-108 dBm |
| TD-SCDMA B34 | 24dBm +1/-3 dBm | <-109 dBm |
| TD-SCDMA B39 | 24dBm +1/-3 dBm | <-109 dBm |
| FDD-LTE B1 (10MHz) | 23dBm+2/-2 dBm | <-97 dBm |

| | | |
|---|---|---|
| FDD-LTE B2 (10MHz) | 23dBm+2/-2 dBm | <-95 dBm |
| FDD-LTE B3 (10MHz) | 23dBm+2/-2 dBm | <-95 dBm |
| FDD-LTE B4(10MHz) | 23dBm+2/-2 dBm | <-97 dBm |
| FDD-LTE B5(10MHz) | 23dBm+2/-2 dBm | <-95 dBm |
| FDD-LTE B7(10MHz) | 23dBm+2/-2 dBm | <-95 dBm |
| FDD-LTE B8(10MHz) | 23dBm+2/-2 dBm | <-95 dBm |
| FDD-LTE B9(10MHz) | 23dBm+2/-2 dBm | <-96 dBm |
| FDD-LTE B12(10MHz) | 23dBm+2/-2 dBm | <-95 dBm |
| FDD-LTE B17(10MHz) | 23dBm+2/-2 dBm | <-95 dBm |
| FDD-LTE B20(10MHz) | 23dBm+2/-2 dBm | <-95 dBm |
| FDD-LTE B28(10MHz) | 23dBm+2/-2 dBm | <-95 dBm |
| TDD-LTE B38(10MHz) | 23dBm+2/-2 dBm | <-97 dBm |
| TDD-LTE B39(10MHz) | 23dBm+2/-2 dBm | <-97 dBm |
| TDD-LTE B40(10MHz) | 23dBm+2/-2 dBm | <-97 dBm |
| TDD-LTE B41(10MHz) | 23dBm+2/-2 dBm | <-95 dBm |

NOTE

All the values above are obtained in the lab environment. In actual applications, there might be a difference because of the network environment.

## 5.4 EMI/EMC Features

**Table 5-4** ESD features

| Testing Point | Contact Discharge | Air Discharge |
|---|---|---|
| V_MAIN | ±8 kV | ±15 kV |
| GND | ±8 kV | ±15 kV |
| ANT | ±8 kV | ±15 kV |
| Cover | ±8 kV | ±15 kV |
| Others | ±2 kV | ±4 kV |

NOTE

When using the N720 Mini PCIe module, ensure that the ground near the fixing holes connects to that of the device to avoid module damage caused by ESD.

# 6 Mechanical Feature

## 6.1 Dimensions

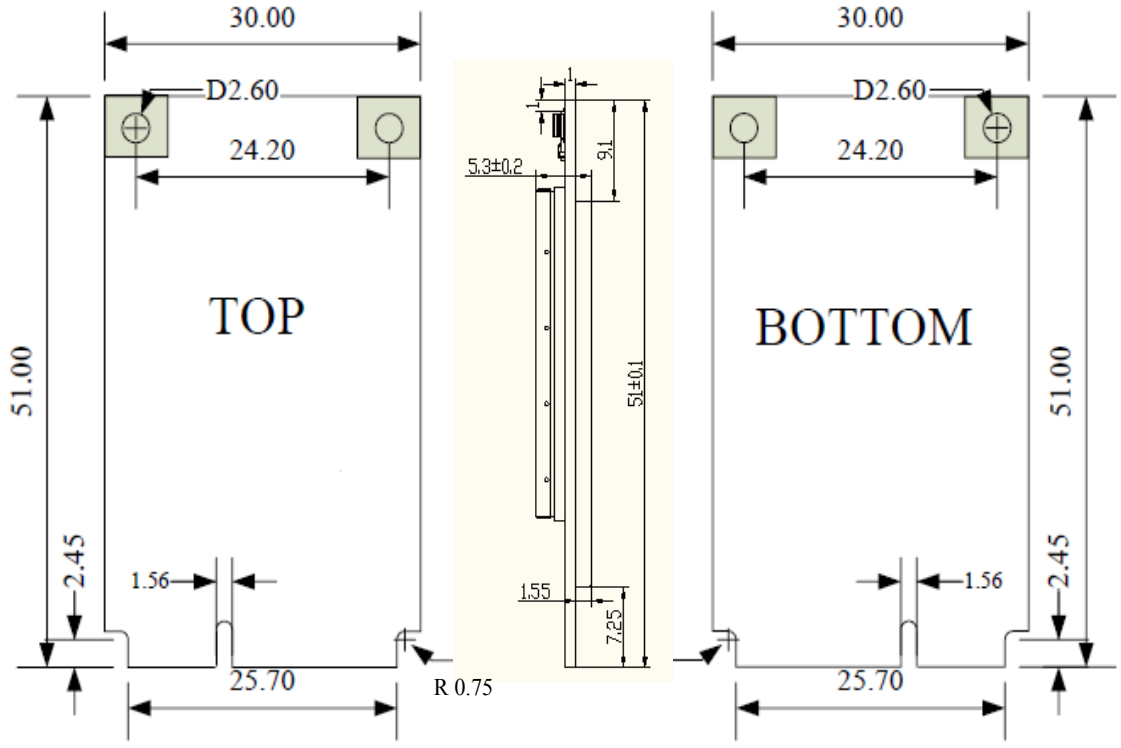
**Table 6-1** N720 dimensions

| Specifications | **N720** |
|---|---|
| Dimensions | (28±0.1) mm x (30±0.1) mm x (2.8±0.1) mm (H x W x D) |
| Weight | 5.1g |
| Package | 100-Pin LGA |

**Table 6-2** N720 Mini PCIe dimensions

| **Specifications** | **N720 Mini PCIe** |
|---|---|
| Dimensions | (30±0.1)mm* (51±0.1) mm* (5.3±0.15)mm (H*W*D) |
| Weight | 11.2g |
| Package | 52-Pin Mini PCIe |

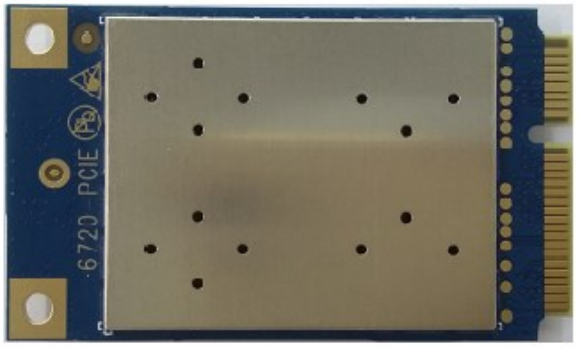
**Figure 6-1** N720 Mini PCIe dimensions



# 6.2 N720 Mini PCIe Pictures

**Figure 6-2** Top view of N720 Mini PCIe


**Figure 6-3** Bottom view of N720 Mini PCIe



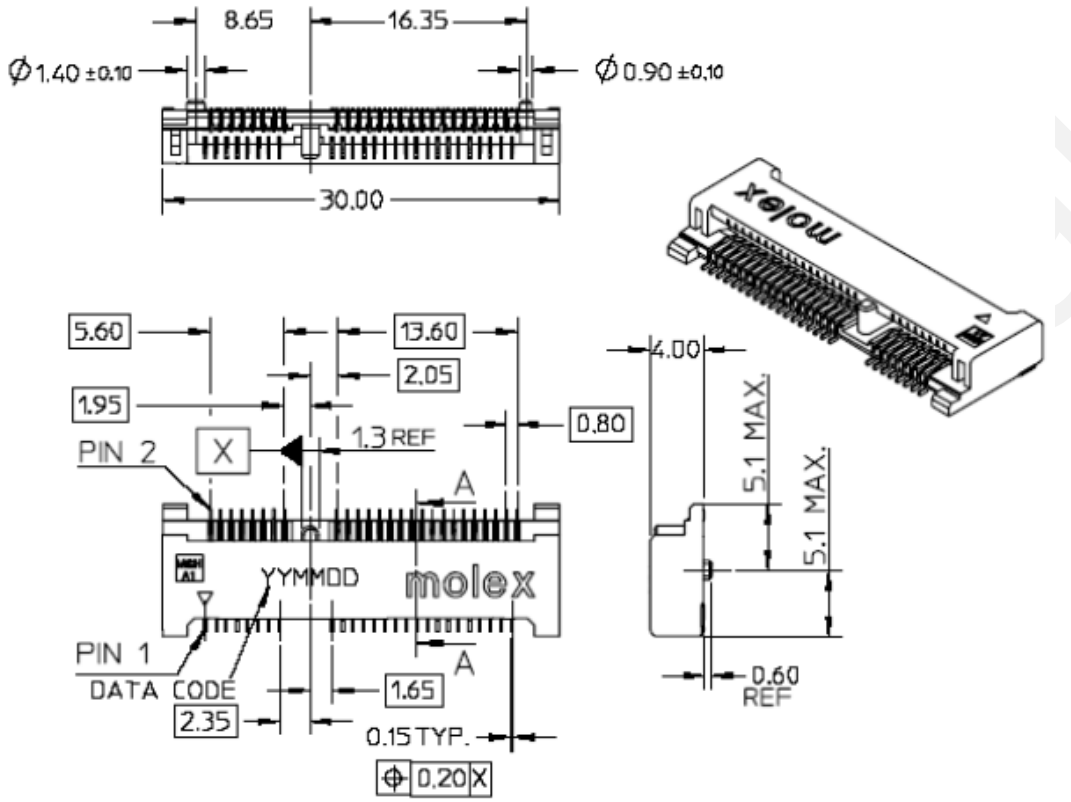

**CAUTION**

The color of the PCB board in the above figures will not be the acceptance criteria.

# 7 Mounting

The N720 Mini PCIe module complies with PCI Express Mini Card 1.2 standard. It is mounted onto the Mini PCIe card connector by plugging in directly. The following figure shows the dimensions of Mini PCIe connector 679100002 from Molex.

**Figure 7-1** Mini PCIe card connector



# 8 Packaging and Storage

## 8.1 Packaging

N720 Mini PCIe modules are packaged using EPE foam tray together with desiccant and humidity indicating card on delivery to guarantee a long shelf life.

**Figure 8-1** N720 Mini PCIe packaging

**Figure 8-2** Shipment packaging


## 8.2 Storage

Storage temperature: 20°C~26°C
Storage humidity: 40%-60%
Storage date: 120 days