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W30 Hardware User Guide

Version 1.0

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GET CONNECTED GET SMART

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Remarks

This document provides guide for users to use the W30.

This document is intended for system engineers (SEs), development engineers, and test engineers.

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Revision Record		
Version	Changes	Date
Version 1.0	Initial draft	2017-09

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1 About W30

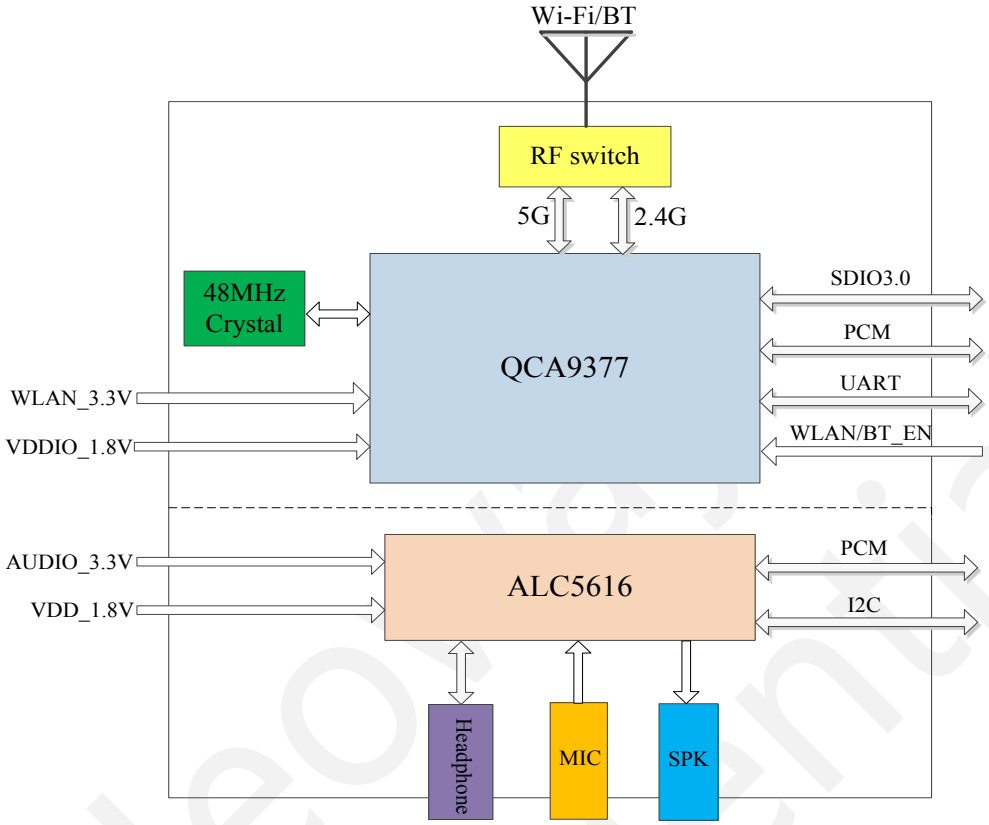
1.1 Overview

W30 is a compact low-power module that supports WLAN, Bluetooth, and Audio. Its dimensions are 20 mm x 18 mm x 2.2 mm. It is developed on Qualcomm QCA9377 chipset and in compliance with the 802.11 standards, so it supports 2.4 GHz and 5 GHz WLAN for high-speed data transmission. The Bluetooth function complies with Bluetooth 4.1 protocol and compatible with earlier versions, and also supports BLE mode. The Audio function is developed on the REALTEK chipset, supports different audio codecs, and provides high-quality audio through various processing interfaces. The module is used with N720 in notebooks, wireless routers/MIFI, Internet of vehicle (IoV), smart home, industrial automation and other equipment.

- QCA9377: WLAN and Bluetooth support low power SDIO 3.0, and UART/PCM interfaces
- Compliant with IEEE 802.11a/b/g/n/ac WLAN protocol, Bluetooth 4.1+HS, compatible with Bluetooth 1.x and Bluetooth 2.x
- Support 2.4GHz and 5GHz WLAN, 80 MHz at most
- Support earphone, SPK, and MIC analog audio interface

1.2 Block Diagram

Figure 1-1 W30 block diagram



1.3 Features

Table 1-1 W30 Features

Specifications	Description
Power supply	3.3V
Idle current	< 20 mA
Current in sleep mode	< 10mA
Temperature	Operating temperature: -25℃ to 85℃
	Storage temperature: -45℃ to +90℃
WLAN feature	SDIO3.0 interface Compliant with 1x1 IEEE802.11a/b/g/n/ac standards Supports 5 GHz 802.11ac and 2.4GHz/5GHz 802.11n Supports 20 MHz, 40MHz@2.4GHz Supports 20 MHz, 40MHz, 80MHz@5GHz Maximum number of APs allowed to access: 15

Bluetooth feature	Supports Bluetooth 4.1, compatible with Bluetooth 4.0, Bluetooth 3.0, Bluetooth 2.x and Bluetooth 1.x Supports GFSK, π/4-DQPSK, 8-DPSK and LE modulation PCM/UART data communication interfaces
Audio feature	PCM data communication interfaces I2C control interface ADC: 94dBA SNR, DAC: 94dBA SNR Two analog audio input: a single-end input, a differential input Two analog audio output: an output without gain, an output with 20 mW gain Adjustable Input/Output volume MIC and SPK analog audio interface Earphone detection
Wireless rate	WLAN 2.4GHz: 802.11b: 1, 2, 5.5, 11Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11n (20MHz): MCS0~MCS7 802.11n (40MHz): MCS0~MCS7 802.11ac: MCS0~MCS9 WLAN 5GHz: 802.11a: 6, 9, 12, 18, 24, 36, 48, 54Mbps 802.11n/ac (20MHz): MCS0~MCS7 802.11n/ac (40MHz): MCS0~MCS7 802.11ac (80MHz): MCS0~MCS9
Antenna feature	1x1 Wi-Fi/Bluetooth antenna interface, 50Ω impedance

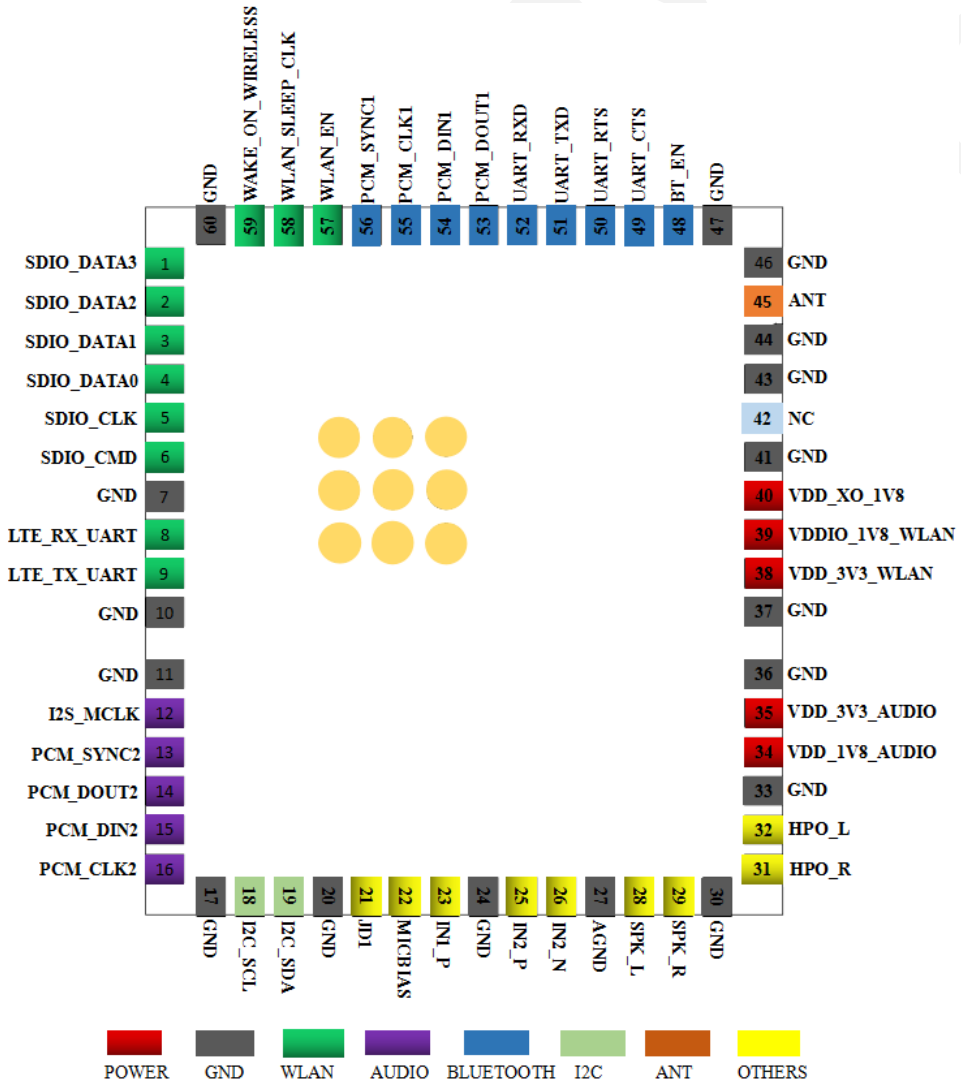
2 Application Interfaces

2.1 Specifications and Pin Definition

Table 2-1 W30 dimensions

Specifications	W30
Dimensions (H x W x D)	(20±0.1 mm) x (18±0.1 mm) x (2.3±0.1 mm)
Weight	1.8g
Package	60-Pin LCC

Figure 2-1 W30 pin description (Top View)



2.2 Pin Description

NOTE

IO: Input/Output DO: Digital output AI: Analog input OD: Output drain

DI: Digital input P: Power supply input AO: Analog output

Table 2-2 W30 pin description

Signal	Pin	I/O	Function	Level Feature	Power Domain	Remarks
Power supply						
VDD_3V3_WLAN	38	P	Main power supply of WLAN	Vmin=3.14V Vmax=3.46V Vtyp=3.3V		The maximum current can be at least 800mA.
VDDIO_1V8_WLAN	39	P	WLAN I/O interface power supply	Vmin=1.71V Vmax=1.9V Vtyp=1.8V		The maximum current can be at least 300mA.
VDD_XO_1V8	40	P	Power supply for WLAN crystal oscillator to pull up	Vmin=1.71V Vmax=1.9V Vtyp=1.8V		Pullup power supply of clock
VDD_3V3_AUDIO	35	P	3.3 V power supply of AUDIO	Vmin=3V Vmax=3.6V Vtyp=3.3V		The maximum current can be at least 300mA.
VDD_1V8_AUDIO	34	P	1.8V power supply of AUDIO	Vmin=1.71V Vmax=1.9V Vtyp=1.8V		1.8 V power supply of audio

GND	7, 10, 37, 41, 43, 44, 46, 47, 60		WLAN/BLUETOOTH ground of the module			
WLAN interface						
SDIO_DATA3	1	IO	SDIO data 3	V_{OL} max=0.45V V_{OH} min=1.35V V_{IL} min=-0.3V V_{IL} max=0.45V V_{IH} min=1.35V V_{IH} max=2.1V	1.8V	Leave this pin unconnected if it is not used.
SDIO_DATA2	2	IO	SDIO data 2			
SDIO_DATA1	3	IO	SDIO data 1			
SDIO_DATA0	4	IO	SDIO data 0			
SDIO_CLK	5	DI	Clock signal of SDIO interface		1.8V	Leave this pin unconnected if it is not used.
SDIO_CMD	6	DI	Control signal of SDIO interface	V_{IL} min=-0.3V V_{IL} max=0.45V V_{IH} min=1.35V V_{IH} max=2.1V	1.8V	Leave this pin unconnected if it is not used.
LTE_RX_UART	8	DI	Co-existing signal of LTE and WLAN, UART data input	V_{IL} min=-0.3V V_{IL} max=0.45V V_{IH} min=1.35V V_{IH} max=2.1V	1.8V	Leave this pin unconnected if it is not used.
LTE_TX_UART	9	DO	Co-existing signal of LTE and WLAN, UART data output	V_{OL} max=0.45V V_{OH} min=1.35V	1.8V	Leave this pin unconnected if it is not used.
WLAN_EN	57	DI	WLAN enable signal	V_{IL} min=-0.3V V_{IL} max=0.45V	1.8V	High level triggers the ON status. Leave this pin unconnected if it is not used.

				V_{IH} min=1.35V V_{IH} max=2.1V		
WLAN_SLEEP_CLK	58	DI	Clock input signal of WLAN in sleep mode.	V_{IL} min=-0.3V V_{IL} max=0.35V V_{IH} min=1.45V V_{IH} max=2V	1.8V	Leave this pin unconnected if it is not used.
WAKE_ON_WIRELESS	59	OD	Control signal of WLAN communication	V_{OL} max=0.45V V_{OH} min=1.35V	1.8V	Leave this pin unconnected if it is not used.
Bluetooth interface						
BT_EN	48	DI	Bluetooth enable	V_{IL} min=-0.3V V_{IL} max=0.45V V_{IH} min=1.35V V_{IH} max=2.1V	1.8V	High level triggers the ON status. Leave this pin unconnected if it is not used.
UART_CTS	49	DI	Clear to send	V_{IL} min=-0.3V V_{IL} max=0.45V V_{IH} min=1.35V V_{IH} max=2.1V	1.8V	Leave this pin unconnected if it is not used.
UART_RTS	50	DO	Request to send	V_{OL} max=0.45V V_{OH} min=1.35V	1.8V	Leave this pin unconnected if it is not used.
UART_TXD	51	DO	UART TX data of the Bluetooth	V_{OL} max=0.45V V_{OH} min=1.35V	1.8V	Leave this pin unconnected if it is not used.
UART_RXD	52	DI	UART RX data of the Bluetooth	V_{IL} min=-0.3V V_{IL} max=0.45V V_{IH} min=1.35V V_{IH} max=2.1V	1.8V	Leave this pin unconnected if it is not used.

PCM_DOUT1	53	DO	PCM data output of the Bluetooth	V_{OL} max=0.45V V_{OH} min=1.35V	1.8V	Leave this pin unconnected if it is not used.
PCM_DIN1	54	DI	PCM data input of the Bluetooth	V_{IL} min=-0.3V V_{IL} max=0.45V V_{IH} min=1.35V V_{IH} max=2.1V	1.8V	Leave this pin unconnected if it is not used.
PCM_CLK1	55	DI	PCM clock signal of the Bluetooth		1.8V	Leave this pin unconnected if it is not used.
PCM_SYNC1	56	IO	PCM frame synchronization signal of the Bluetooth	V_{OL} max=0.45V V_{OH} min=1.35V V_{IL} min=-0.3V V_{IL} max=0.45V V_{IH} min=1.35V V_{IH} max=2.1V	1.8V	Leave this pin unconnected if it is not used.
AUDIO interface						
I2S_MCLK	12	DI	Input signal of I2S main clock		1.8V	Leave this pin unconnected if it is not used.
PCM_SYNC2	13	IO	PCM frame synchronization signal of the AUDIO	V_{OL} max=0.45V V_{OH} min=1.35V V_{IL} min=-0.3V V_{IL} max=0.45V V_{IH} min=1.35V V_{IH} max=2.1V	1.8V	Leave this pin unconnected if it is not used.
PCM_DOUT2	14	DO	PCM data output of the AUDIO	V_{OL} max=0.45V V_{OH} min=1.35V	1.8V	Leave this pin unconnected if it is not used.
PCM_DIN2	15	DI	PCM data output of the	V_{IL} min=-0.3V	1.8V	Leave this pin unconnected if it is

			AUDIO	V_{IL} max=0.45V V_{IH} min=1.35V V_{IH} max=2.1V		not used.
PCM_CLK2	16	IO	PCM clock signal of the AUDIO	V_{OL} max=0.45V V_{OH} min=1.35V V_{IL} min=-0.3V V_{IL} max=0.45V V_{IH} min=1.35V V_{IH} max=2.1V	1.8V	Leave this pin unconnected if it is not used.
I2C_SCL	18	DI	Input signal of I2C clock	V_{IL} min=-0.3V V_{IL} max=0.45V V_{IH} min=1.35V V_{IH} max=2.1V	1.8V	Add a pull-up resistor externally. Leave this pin unconnected if it is not used.
I2C_SDA	19	IO	I2C data signal	V_{OL} max=0.45V V_{OH} min=1.35V V_{IL} min=-0.3V V_{IL} max=0.45V V_{IH} min=1.35V V_{IH} max=2.1V	1.8V	
JD1	21	DI	Earphone detection	3 types of level detectable (threshold): V_{t1}=1.485V V_{t2}=1.925V V_{t3}=2.7V		Leave this pin unconnected if it is not used.
MICBIAS	22	DO	Provides MIC bias voltage	Vtyp=3.3V		Leave this pin unconnected if it is not used.

IN1_P	23	AI	Single-end MIC input			Leave this pin unconnected if it is not used.
IN2_P	25	AI	Positive signal of the MIC	Differential input		Leave this pin unconnected if it is not used.
IN2_N	26	AI	Negative signal of the MIC			
SPK_L	28	AO	Positive signal of the SPK	Differential input		Leave this pin unconnected if it is not used.
SPK_R	29	AO	Negative signal of the SPK			
HPO_R	31	AO	Right sound channel of the earphone output			Leave this pin unconnected if it is not used.
HPO_L	32	AO	Left sound channel of the earphone output			
GND	11, 17, 20, 24, 30, 33, 36		AUDIO ground			The trace layout should be separated from the ground for WLAN/BLUETOOTH.
AGND	27		Analog ground			Connected to the AUDIO ground and main ground. Ensure that the contact area of the connection between this pin and the main ground is big enough.
Other Interfaces						
ANT	45		Wi-Fi/Bluetooth antenna pin			50 Ω impedance
NC	42					NC

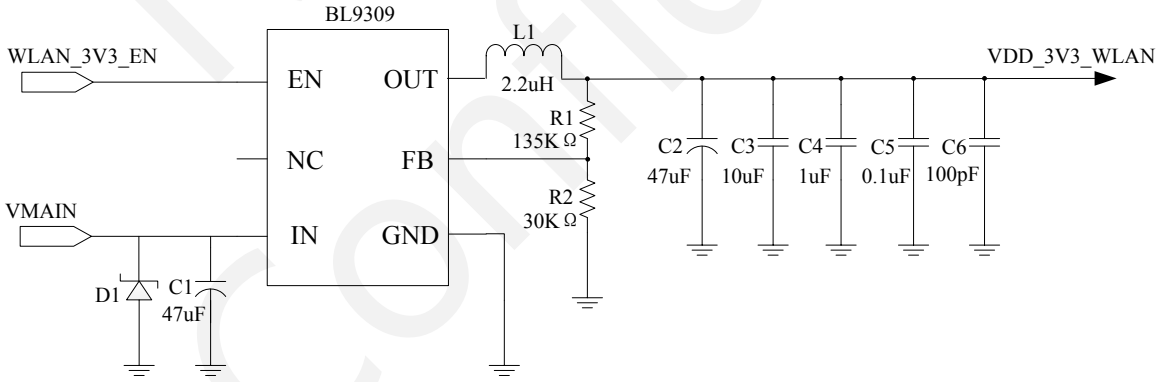
2.3 Power Supply Pins

Signal	Pin	I/O	Function	Remarks
VDD_3V3_WLAN	38	P	Main power supply of WLAN	The maximum current can be at least 800 mA.
VDDIO_1V8_WLAN	39	P	WLAN I/O interface power supply	The maximum current can be at least 300 mA.
VDD_XO_1V8	40	P	Power supply for WLAN crystal oscillator to pull up	Power supply for the crystal oscillator clock to pull up
VDD_3V3_AUDIO	35	P	3.3 V power supply of AUDIO	The maximum current can be at least 300 mA.
VDD_1V8_AUDIO	34	P	Power supply for AUDIO I/O interface	1.8 V power supply of audio

2.3.1 Design of WLAN Power Supply

VDD_3V3_WLAN is the main power supply input pin for the Wi-Fi function of the module. Its input voltage ranges from 3.14 V to 3.46 V and the typical value is 3.3 V. It is recommended that the maximum input current of the external power supply chipset should be at least 800 mA, which can fulfill the requirements for current in all kinds of work modes. The power supply is a critical path to module's performance and stability. The reference design of the WLAN power supply is shown as below:

Figure 2-2 Reference design of 3.3 V WLAN power supply

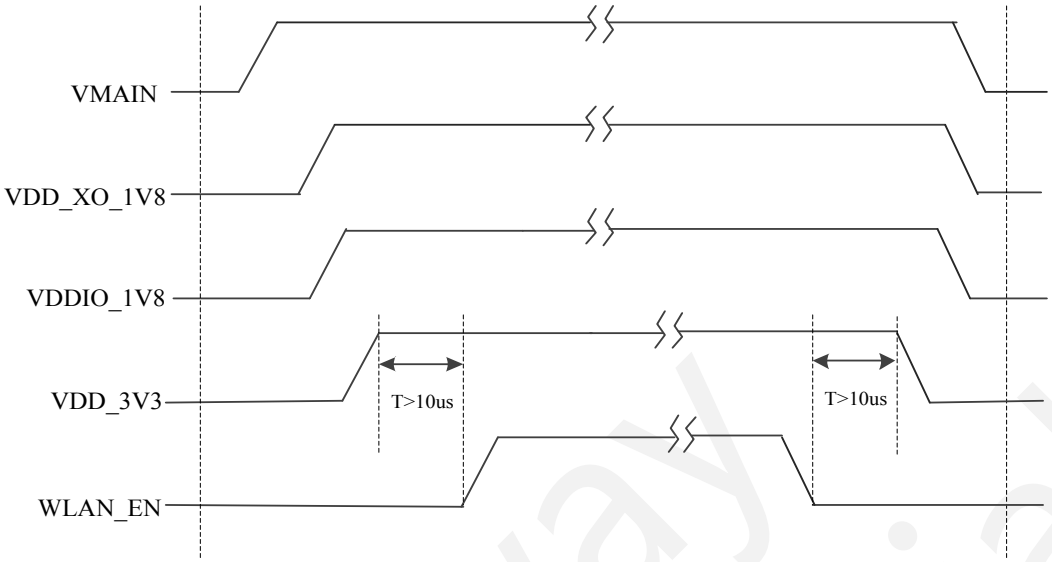


In Figure 2-2, use TVS at D1 to enhance the performance of the module during a burst. SMF5.0AG is recommended. A large bypass tantalum capacitor (47 µF) is expected at C2 to reduce voltage drops during bursts together with C3 (10 µF ceramics capacitor). In addition, add 0.1 µF and 100 pF filter capacitors to enhance the stability of the power supply.

VDDIO_1V8_WLAN and VDD_XO_1V8 are respectively the internal I/O power supply of the module and the pullup power supply of the WLAN crystal oscillator. The level of VDDIO must be same as the I/O level of the host, and the maximum work current should be at least 300 mA.

Figure 2-3 shows the power on/off sequence of the WLAN.

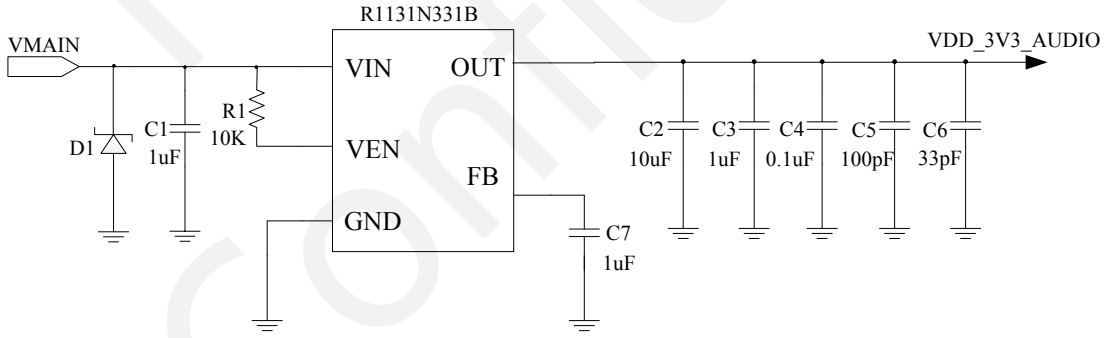
Figure 2-3 Power on/off sequence of the WLAN



2.3.2 Design of AUDIO Power Supply

VDD_3V3_AUDIO is the main power supply input pin for the AUDIO function of the module. Its input voltage ranges from 3.0 V to 3.6 V and the typical value is 3.3 V. It is recommended that the maximum input current of the power supply should be at least 300 mA, which can fulfill the current requirements of the AUDIO function. The reference design of the AUDIO power supply is shown as below:

Figure 2-4 Reference design of AUDIO power supply



VDD_1V8_AUDIO provides 1.8 V power supply input for the AUDIO and loads a very low current. The external 1.8 V voltage is introduced into logic inputs to pull up the internal IO interface.

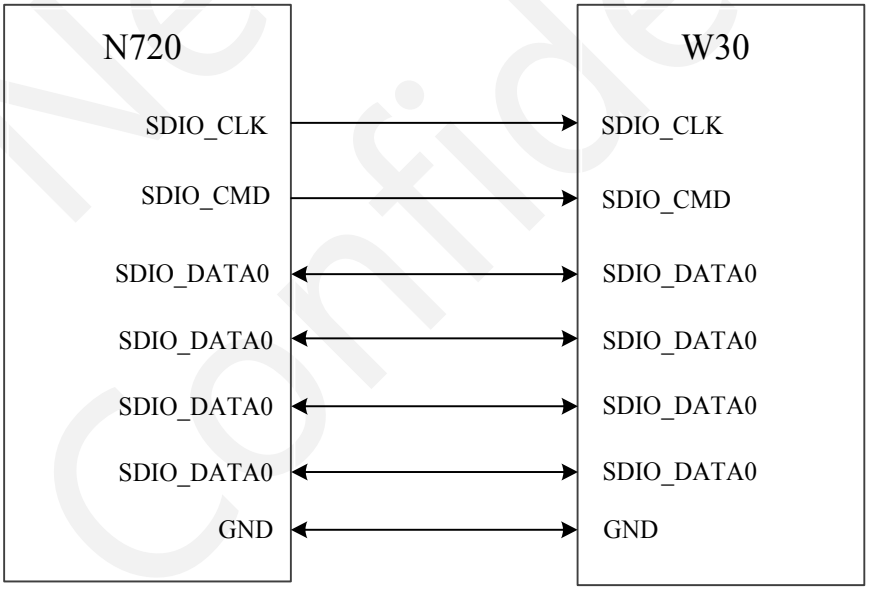
2.4 WLAN Application Interfaces

2.4.1 SDIO Interface

Signal	Pin	I/O	Function	Remarks
SDIO_DATA3	1	IO	SDIO data 3	Leave this pin unconnected if it is not used.
SDIO_DATA2	2	IO	SDIO data 2	Leave this pin unconnected if it is not used.
SDIO_DATA1	3	IO	SDIO data 1	Leave this pin unconnected if it is not used.
SDIO_DATA0	4	IO	SDIO data 0	Leave this pin unconnected if it is not used.
SDIO_CLK	5	DI	Clock signal of SDIO interface	Leave this pin unconnected if it is not used.
SDIO_CMD	6	DI	Control signal of SDIO interface	Leave this pin unconnected if it is not used.

The WLAN function of the W30 module complies with 8-bit SDIO 3.0 Interface Protocol, and supports 802.11ac 256-QAM modulation. The transmission rate of the WLAN TCP/IP can reach 215 Mbps at an 80 MHz bandwidth. Figure 2-5 shows the SDIO connection between W30 and N720.

Figure 2-5 SDIO connection



CLK, CMD, DATA0, DATA1, DATA2 and DATA3 are high-speed signal lines. Limit their characteristic impedance to 50Ω and do not allow them to cross any other traces. Ensure length matching for CMD, DATA0, DATA1, DATA2 and DATA3 traces. CLK trace should be grounded separately.

2.4.2 WLAN Control Interface

Signal	Pin	I/O	Function	Remarks
LTE_RX_UART	8	DI	Co-existing signal of LTE and WLAN, UART data input	It is pulled up internally. Leave this pin unconnected if it is not used.
LTE_TX_UART	9	DO	Co-existing signal of LTE and WLAN, UART data output	Leave this pin unconnected if it is not used.
WLAN_EN	57	DI	WLAN enable signal	High level triggers the ON status. Leave this pin unconnected if it is not used.
WLAN_SLEEP_CLK	58	DI	Clock signal of WLAN in sleep mode.	Leave this pin unconnected if it is not used.
WAKE_ON_WIRELESS	59	OD	Control signal of WLAN communication	Leave this pin unconnected if it is not used.

LTE_RX_UART and LTE_TX_UART are co-existing signals of LTE and Wi-Fi and can be used to send and receive UART data.

WLAN_EN is the signal to enable or disable the Wi-Fi function. It is pulled down internally and a high level trigger. For its power on/off sequence, see Figure 2-3.

WLAN_SLEEP_CLK is the clock input signal of the Wi-Fi function in sleep mode. The clock frequency is 32.768 KHz. When the WLAN function enters sleep mode, an external 32.768 KHz clock signal is required to wake up the module from different modes for data receiving. Figure 2-6 shows the sequence of the 32 KHz clock signal. Table 2-3 lists the parameters.

Figure 2-6 Sequence of 32 KHz clock signal

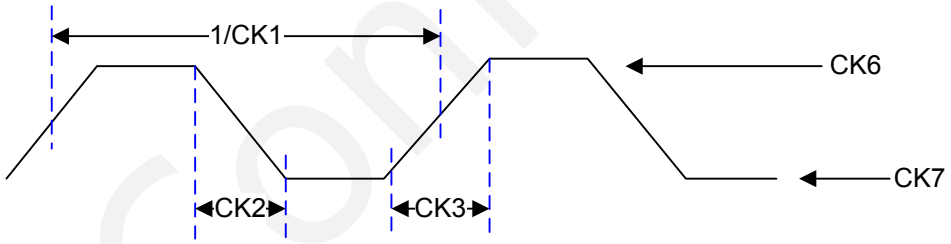


Table 2-3 Parameters of 32 KHz clock signal sequence

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Clock frequency	CK1	-	32.768	-	kHz
Fall time	CK2	1	-	100	ns
Rise time	CK3	1	-	100	ns
Duty ratio	CK4	15	-	85	%
Frequency error	CK5	-200	-	200	ppm
Input high level	CK6	1.45	-	2	V

Input low level	CK7	-0.3	-	0.35	V

WAKE_ON_WIRELESS is the communication control signal in WLAN mode. Operating at 1.8 V, this pin is an open-drain output.

2.5 Bluetooth Application Interfaces

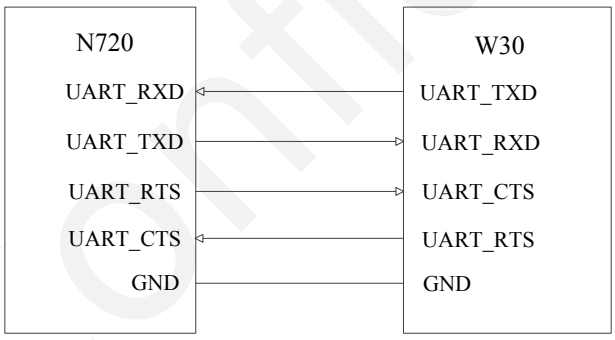
The Bluetooth function is implemented mainly by the UART and PCM data communication interfaces and the BT_EN control signal.

2.5.1 Bluetooth UART Interface

Signal	Pin	I/O	Function	Remarks
UART_CTS	49	DI	Clear to send	Leave this pin unconnected if it is not used.
UART_RTS	50	DO	Request to send	Leave this pin unconnected if it is not used.
UART_TXD	51	DO	UART TX data of the Bluetooth	Leave this pin unconnected if it is not used.
UART_RXD	52	DI	UART RX data of the Bluetooth	Leave this pin unconnected if it is not used.

The Bluetooth function of W30 requires one complete UART interface, which supports flow control and operates at 1.8V. Figure 2-7 shows the UART connection.

Figure 2-7 UART connection



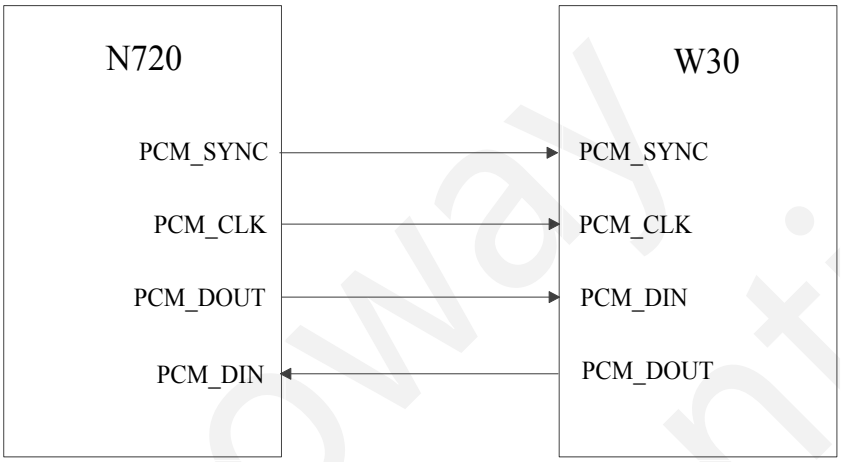
2.5.2 BLUETOOTH PCM Interface

Signal	Pin	I/O	Function	Remarks
PCM_DOUT1	53	DO	PCM data output of the Bluetooth	Leave this pin unconnected if it is not used.
PCM_DIN1	54	DI	PCM data input of the Bluetooth	Leave this pin unconnected if it is not used.
PCM_CLK1	55	DI	PCM clock signal of the Bluetooth	Leave this pin unconnected if it is

				not used.
PCM_SYNC1	56	IO	PCM frame synchronization signal of the Bluetooth	Leave this pin unconnected if it is not used.

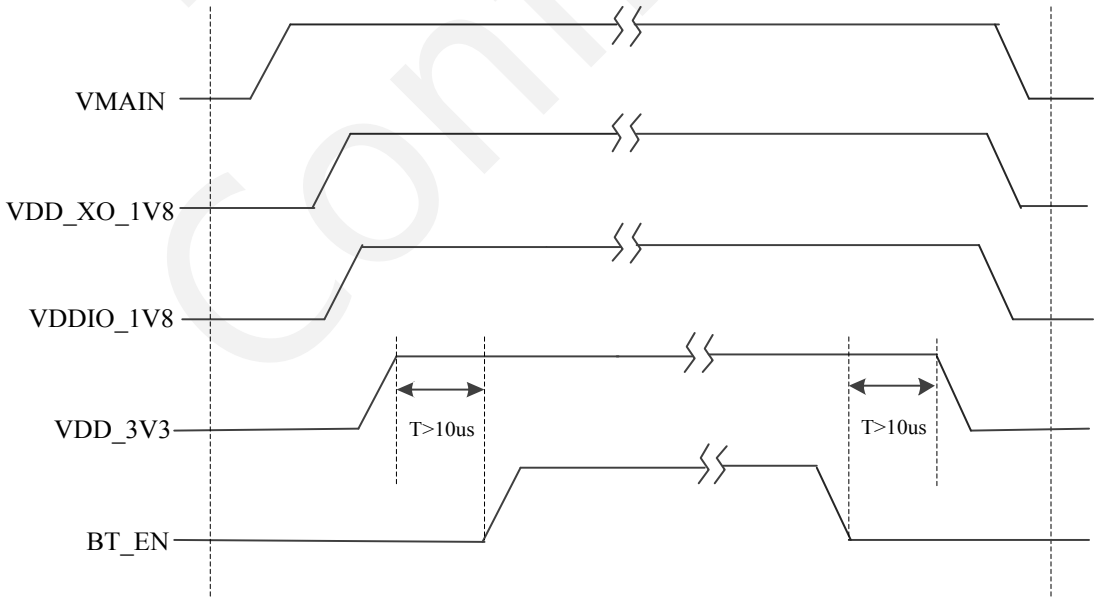
In addition to UART interface, the Bluetooth requires a PCM interface, which operates at 1.8 V. Figure 2-8 shows the PCM connection.

Figure 2-8 PCM connection



The BT_EN signal controls the switch of the Bluetooth function. It is pulled down internally and triggered by high level. Figure 2-9 shows the power on/off sequence of the Bluetooth.

Figure 2-9 Power on/off sequence of the Bluetooth



2.6 AUDIO Application Interfaces

AUDIO interfaces include PCM, I2C, and analog audio interface.

2.6.1 Audio PCM Interface

Signal	Pin	I/O	Function	Remarks
PCM_SYNC2	13	IO	AUDIO PCM sync signal	Leave this pin unconnected if it is not used.
PCM_DOUT2	14	DO	PCM data output of the Bluetooth	Leave this pin unconnected if it is not used.
PCM_DIN2	15	IO	PCM data input of the AUDIO	Leave this pin unconnected if it is not used.
PCM_CLK2	16	IO	PCM clock signal of the AUDIO	Leave this pin unconnected if it is not used.
I2S_MCLK	12	DI	Input signal of I2S main clock	Leave this pin unconnected if it is not used.

The AUDIO function of W30 communicates through one PCM interface. It supports both host and device modes and operates at 1.8 V. Figure 2-10 and Figure 2-11 shows the PCM sequence respectively in host and device modes.

Figure 2-10 PCM sequence in host mode

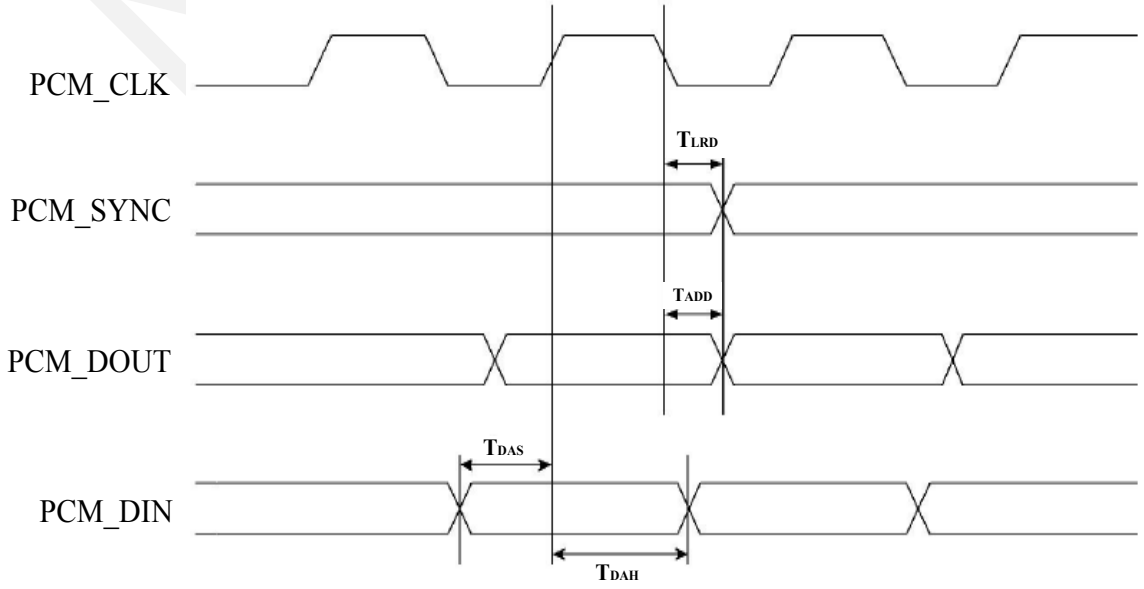


Table 2-4 Parameters of PCM sequence in host mode

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Delay between frame synchronization and	TLRD	-	-	30	ns

clock signal					
Delay between data output and clock signal	T_{ADD}	-	-	30	ns
Time period that data input signal is set up	T_{DAS}	10	-	-	ns
Time period that data input signal lasts	T_{DAH}	10	-	-	ns

Figure 2-11 PCM sequence in device mode

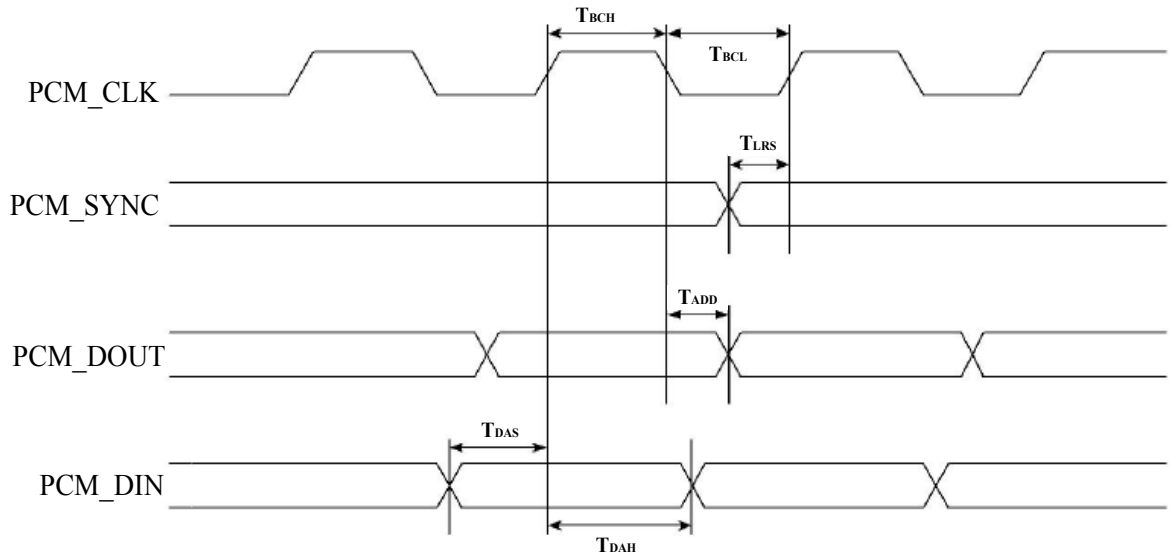


Table 2-5 Parameters of PCM sequence in device mode

Parameter	Symbol	Minimum	Typical	Maximum	Unit
BCKO pulse width high	T_{BCH}	20	-	-	ns
BCKO pulse width low	T_{BCL}	20	-	-	ns
Time period that synchronization input signal is set up	T_{LRS}	30	-	-	ns
Delay between data output and clock signal	T_{ADD}	-	-	30	ns
Time period that data input signal is set up	T_{DAS}	10	-	-	ns
Time period that data input signal lasts	T_{DAH}	10	-	-	ns

I2S_MCLK is the main clock signal referred by the system clock of the AUDIO. When PCM_CLK is configured as clock signal output in host mode, I2S_MCLK is configured as the main clock signal of the system. When PCM_CLK is configured as clock signal input in device mode, PCM_CLK signal should be synchronous with I2S_MCLK signal.

2.6.2 AUDIO I2C Interface

Signal	Pin	I/O	Function	Remarks
I2C_SCL	18	DI	Input signal of I2C clock	Add a pull-up resistor externally. Leave this pin

I2C_SDA	19	IO	I2C data signal	unconnected if it is not used.

The AUDIO function of W30 allows one I2C interface to be control signal. The maximum rate at the I2C interface can be 3.4 Mbps and the interface operates at high level 1.8 V. Add a pull-up resistor externally. Figure 2-12 shows the reference design of the I2C interface.

Figure 2-12 Reference design of the I2C interface

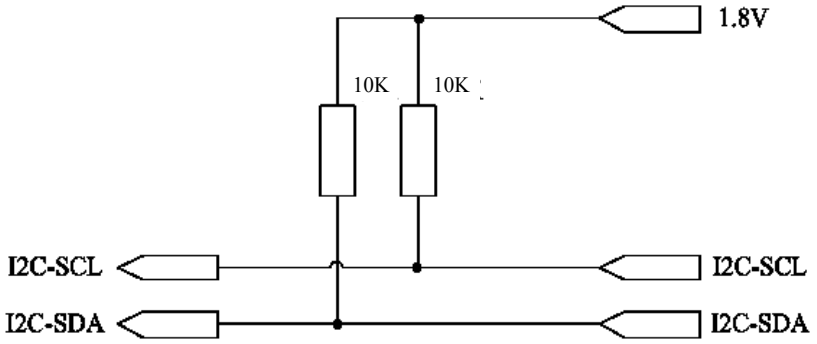


Figure 2-13 shows the sequence of the I2C control signal.

Figure 2-13 I2C interface sequence

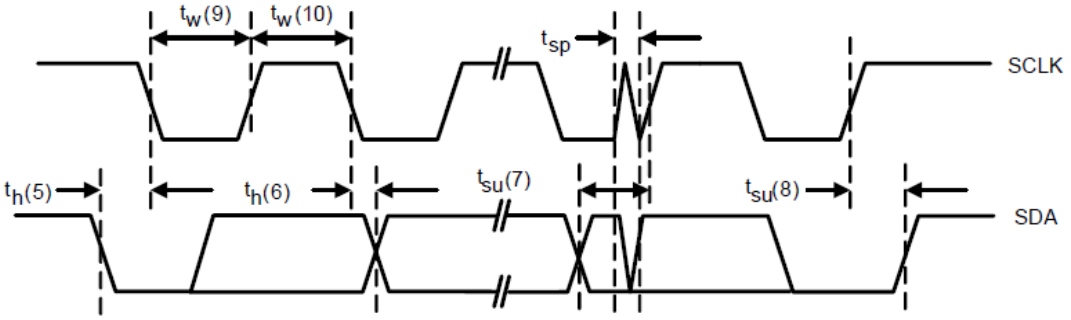


Table 2-6 I2C sequence parameters

Parameter	Symbol	Minimum	Typical	Maximum	Unit
BCKO pulse width low	$t_w(9)$	1.3	-	-	us
BCKO pulse width high	$t_w(10)$	600	-	-	ns
Clock frequency	F	0	-	400K	Hz
Time period that the signal lasts	$t_h(5)$	600	-	-	ns
Time period that data input signal is set up	$t_{su}(7)$	100	-	-	ns
Time period that data input signal lasts	$t_h(6)$	-	-	900	ns
Close signal setup time	$t_{su}(8)$	600	-	-	ns
Width that filter suppresses peak pulse	t_{sp}	0	-	50	ns

2.6.3 Analog Audio interface

Signal	Pin	I/O	Function	Remarks
JD1	21	DI	Earphone detection	3 types of level detectable (threshold): V_{t1}=1.485V; V_{t2}=1.925V; V_{t3}=2.7V
MICBIAS	22	DO	Provides MIC bias voltage	Leave this pin unconnected if it is not used.
IN1_P	23	AI	Single-end MIC input	Leave this pin unconnected if it is not used.
IN2_P	25	AI	Positive signal of the MIC	Leave this pin unconnected if it is not used.
IN2_N	26	AI	Negative signal of the MIC	Leave this pin unconnected if it is not used.
SPK_L	28	AO	Positive signal of the SPK	Leave this pin unconnected if it is not used.
SPK_R	29	AO	Negative signal of the SPK	Leave this pin unconnected if it is not used.
HPO_R	31	AO	Right sound channel of the earphone output	Leave this pin unconnected if it is not used.
HPO_L	32	AO	Left sound channel of the earphone output	Leave this pin unconnected if it is not used.
AGND	27		Analog ground	It is connected to the main GND. Leave this pin unconnected if it is not used.

The analog audio function is implemented mainly by the Headphone interface, the MIC interface, and the SPK interface.

Headphone Interface

The headphone interface uses the JD1, MICBIAS, IN1_P, HPO_R, and HPO_L pins. This interface can detect headphone automatically and the volume can be adjusted by AT commands. Figure 2-14 shows the reference design of headphone circuit.

Figure 2-14 Reference design of headphone

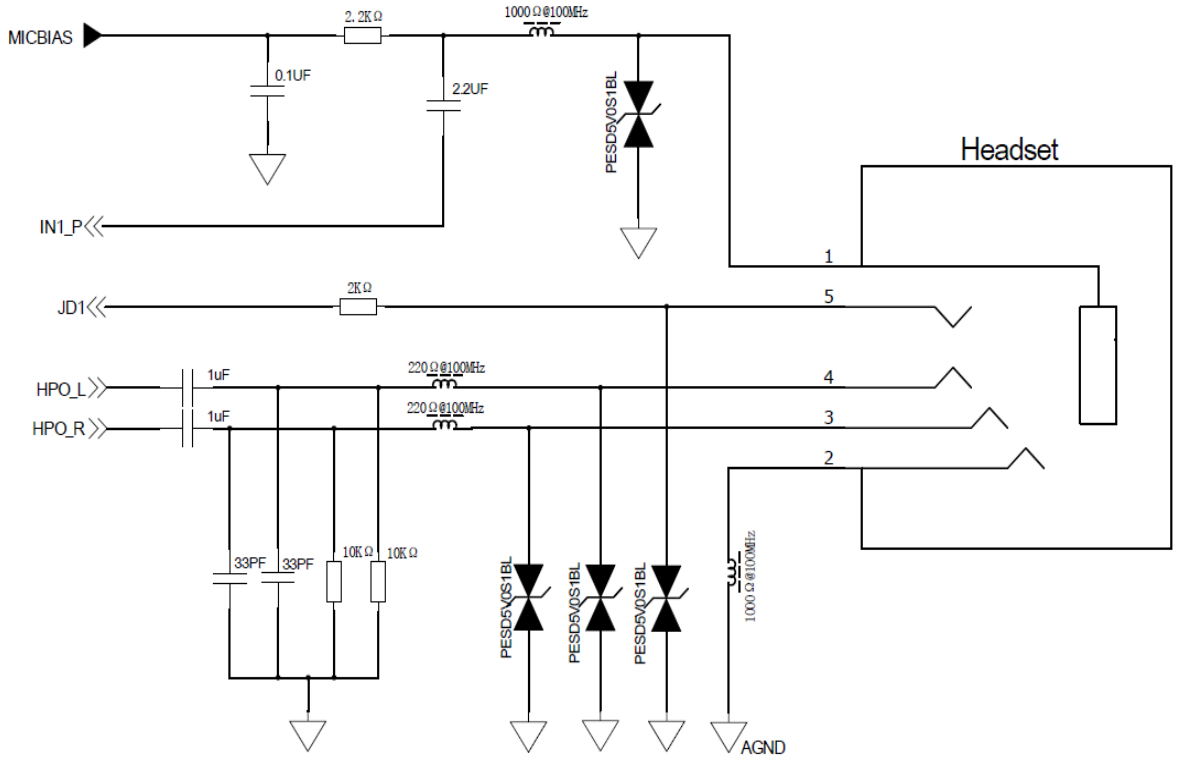
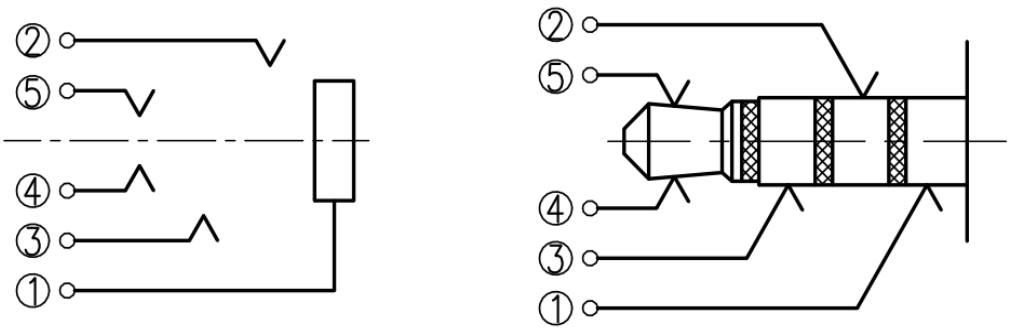


Figure 2-15 Headphone interface



Please note if the headphone is CTIA or OMTP. The connections of ①and ② are reverse for the two type of headphones. The JD1 pin (⑤ in the above figure) is unconnected if the headphone is not plugged. After the headphone is plugged, this pin is connected to GND through the left channel (8/16/32 Ω) loudspeaker of the headphone.

Differential MIC/SPK Interface

MIC_P and MIC_N are the differential signals of MIC. Generally condenser microphone is recommended.

SPK_P and SPK_N are the differential signals of speaker. The volume of MIC and SPK can be adjusted through AT commands. For details, see the Neoway_N720_Wi-Fi_AUDIO_Application_Guide_V1.0.

Figure 2-16 shows the reference design of the MIC circuit.

Figure 2-16 Reference design of the MIC circuit

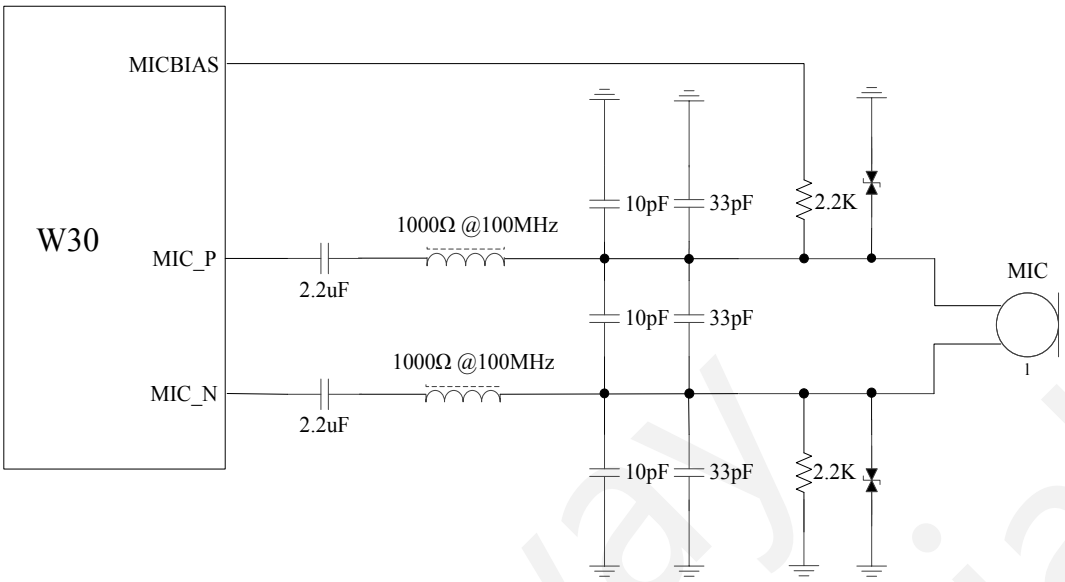


Figure 2-17 shows the reference design of the receiver circuit.

Figure 2-17 Reference design of the receiver circuit

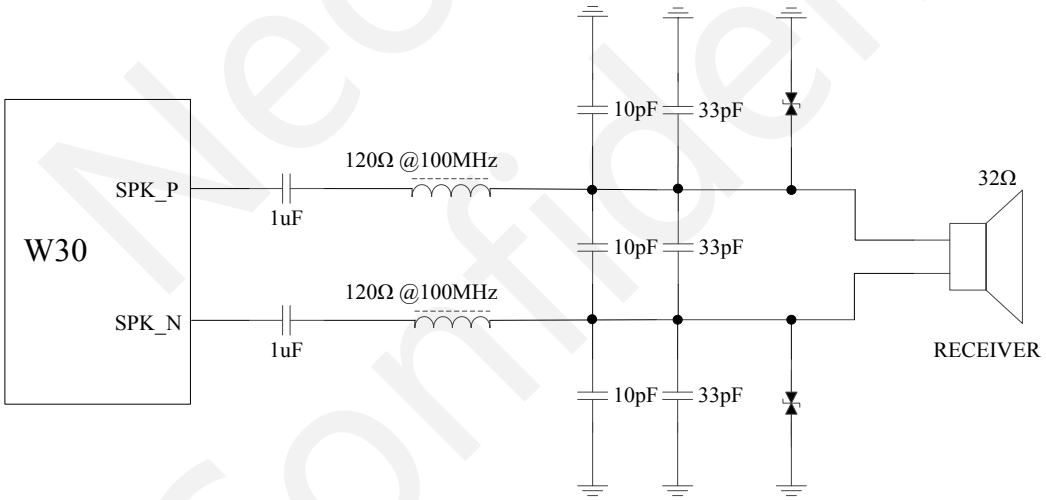
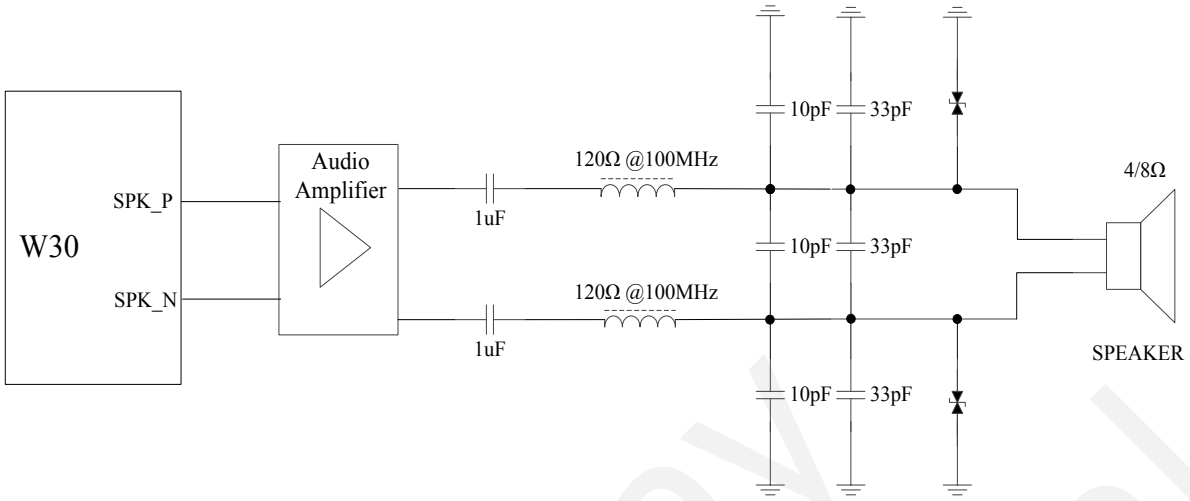


Figure 2-18 shows the reference design of the speaker circuit.

Figure 2-18 Reference design of the speaker circuit



Audio Design Cautions

- On the PCB board, beed, filter capacitors, ESD components should be placed as close to the audio components as possible.
- Traces should be as short as possible and be far away from antenna and power supply.
- Differential traces should follow the design rules.
- The audio signal traces should be wide enough on the PCB to bear large current when the module output audios at the highest volume.
- The traces should be isolated from digital signals and clock as well as other analog signal traces. No signal trace crossing is allowed. Reserve enough grounding holes and ground protection.
- Do not connect the audio output pins to GND.

3 RF Interface

Signal	Pin	I/O	Function	Remarks
ANT	45	AI/O	Wi-Fi/Bluetooth antenna	50Ω impedance

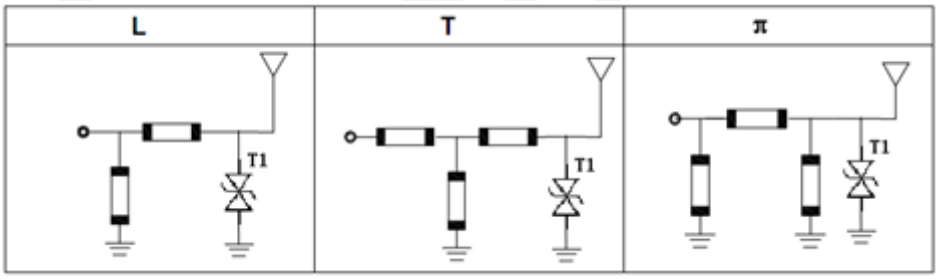
The 45th pin of W30 is the Wi-Fi/Bluetooth antenna interface and the impedance is 50 Ω. It can connect to 2.4G/5G ceramic chip antenna or magnetic antenna. The antenna should be well matched to achieve best performance. It should be installed far away from high speed logic circuits, DC/DC power, or any other strong disturbing sources if developers use RF cable to connect.

It is recommended to add an ESD protection diode to the antenna interface in an environment with great electromagnetic interference and other applications with bad ESD. The ESD protection diode must have ultra-low capacitance (lower than 0.5 pF). Otherwise, it will affect the impedance of the RF loop or result in attenuation of RF signals. RCLAMP0521P from Semtech or ESD5V3U1U from Infineon is recommended.

In PCB design, the RF trace between the antenna pad of module and the antenna connector, should have a 50 Ω characteristic impedance, and be as short as possible. The trace should be surrounded by ground copper. The distance between the RF traces and ground copper should be twice of the RF trace width. Dig as many ground holes as possible on the copper to ensure lowest grounding impedance.

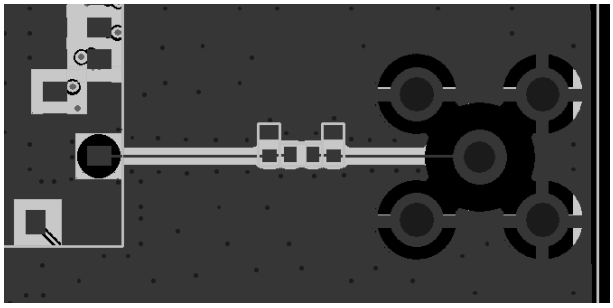
If the trace between the module and connector has to be longer, or built-in antenna is used, a matching circuit is needed, as shown in the following figure.

Figure 3-1 Reference design of antenna matching



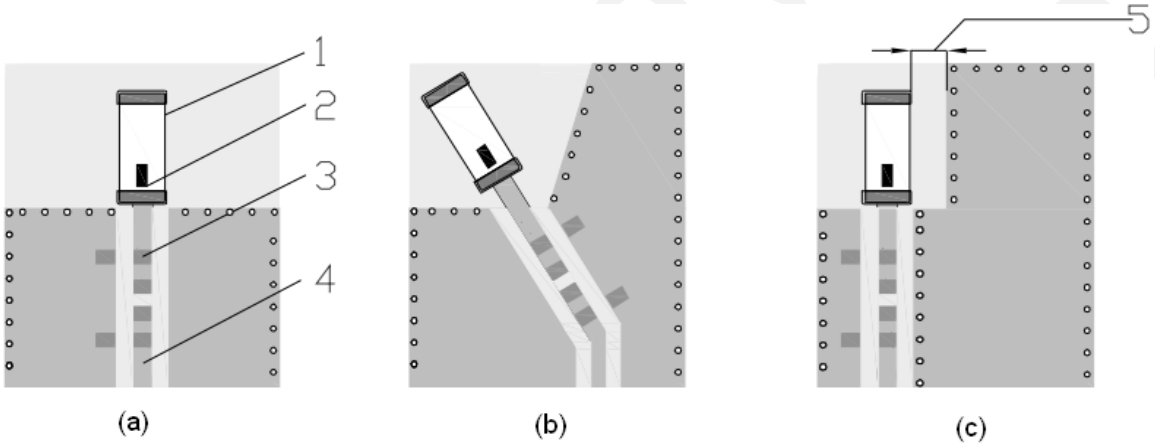
T1 in the figure is an ESD diode (optional). Developers can choose one type of the matching circuits in the figure. The π-type is recommended. Big RF solder pad can result in great parasitic capacitance, which will affect the antenna performance. Remove the copper on the first and second layers under the RF solder pad.

Figure 3-2 Recommended RF PCB design



Refer to the following antenna layouts if a ceramic chip antenna is used.

Figure 3-3 Antenna layout



1: Ceramic chip antenna

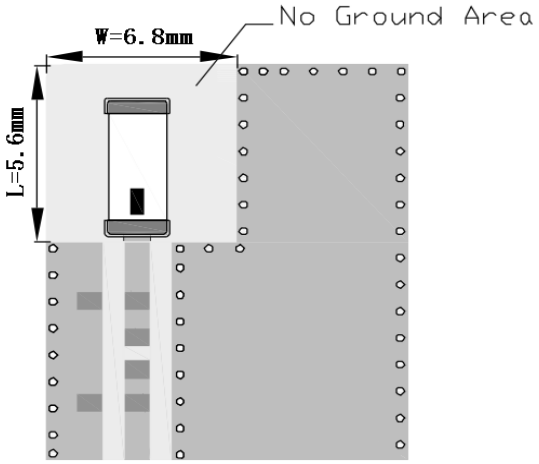
2: Feeder

3: Pad of the matching circuit

4: 50Ω transmission line

The first type of antenna layout is recommended if the PCB is big enough. Number 5 in Figure 3-3 shows the area between the antenna and the ground Figure 3-4 shows the clearance if this area.

Figure 3-4 Clearance around the antenna



CAUTION

On the PCB, keep the RF signals and RF components away from high-speed circuits, power supplies, transformers, inductors, the clock circuit of MCU, etc.

4 Electric Feature and Reliability

4.1 Electric Feature

Table 4-1 W30 Electric Feature

Module Status		Minimum Value	Typical Value	Maximum Value
WLAN_3.3V	Vin	3.135 V	3.3 V	3.465 V
	Iin	-	-	800 mA
AUDIO_3.3V	Vin	3 V	3.3 V	3.6 V
	Iin	-	-	300 mA

CAUTION

- If the voltage is too low, the WLAN/Bluetooth or AUDIO function might not work properly. If the voltage is too high or there is a voltage burst during the startup, the module might be damaged permanently.
- If using LDO or DC-DC to supply power for the module, ensure that it outputs a rated current.

4.2 Temperature Feature

Table 4-2 W30 Temperature Feature

Module Status	Minimum Value	Typical Value	Maximum Value
Operating temperature	-25℃	25℃	85℃
Storage temperature	-45℃	-	90℃

CAUTION

If the module works at a temperature exceeding the thresholds, its RF performance of Wi-Fi or Bluetooth might be worse and the audio function does not work properly.

4.3 ESD Protection

Electronics need to pass several ESD tests. The following table shows the ESD capability of key pins of this module. It is recommended to add ESD protection based on the application to ensure product quality when designing a product.

Table 4-3 W30 ESD protection

Testing Point	Contact Discharge	Air Discharge
Power supply pins	±8 kV	±15 kV
GND	±8 kV	±15 kV
ANT	±8 kV	±15 kV
Cover	±8 kV	±15 kV
Others	±2 kV	±4 kV

NOTE

Testing environment: Humidity 45%; Temperature 25℃

5 RF Feature

5.1 Work Band

Table 5-1 Work band

Work band	Parameter	Frequency
WLAN 2.4 GHz	Center channel frequency	2412~2484 MHz
WLAN 5GHz	Center channel frequency	4900~5925 MHz
Bluetooth	Center channel frequency	2402~2480 MHz

5.2 TX Power and RX Sensitivity

Table 5-2 Wi-Fi/Bluetooth TX power and RX sensitivity

Work Band	Rate	Transmit Power	Receiving Sensitivity
802.11b (2.4G)	1/2/5.5/11Mbps	15 dBm	-75 dBm
802.11g (2.4G)	6/9/12/18/24/36Mbps	14 dBm	-75 dBm
	48/54Mbps	13.5 dBm	-70 dBm
802.11n (2.4G, 20MHz)	MCS0~MCS4	14 dBm	-70 dBm
	MCS5~MCS7	13.5 dBm	-65 dBm
802.11n (2.4G, 40MHz)	MCS0~MCS4	13.5 dBm	-67 dBm
	MCS5~MCS7	12.5 dBm	-60 dBm
802.11ac (2.4G, 20MHz)	MCS8	12 dBm	-57 dBm
802.11ac (2.4G, 40MHz)	MCS9	11 dBm	-55 dBm
802.11a (5G)	6/9/12/18/24Mbps	12 dBm	-74 dBm
	36/48Mbps	11 dBm	-67 dBm
	54Mbps	10 dBm	-65 dBm
802.11n/ac (5G, 20MHz)	MCS0~MCS2	12 dBm	-76 dBm
	MCS3~MCS5	11 dBm	-65 dBm
	MCS6~MCS7	9.5 dBm	-62 dBm
802.11n/ac (5G, 40MHz)	MCS0~MCS2	11 dBm	-75 dBm
	MCS3~MCS6	10 dBm	-62 dBm
	MCS7	9 dBm	-60 dBm
802.11ac (5G, 80MHz)	MCS8~MCS9	6.5 dBm	-50 dBm

Bluetooth	GFSK	8 dBm	-92 dBm
	π/4-DQPSK	7 dBm	-92 dBm
	8-DPSK	7 dBm	-85 dBm
	LE	3 dBm	-95 dBm

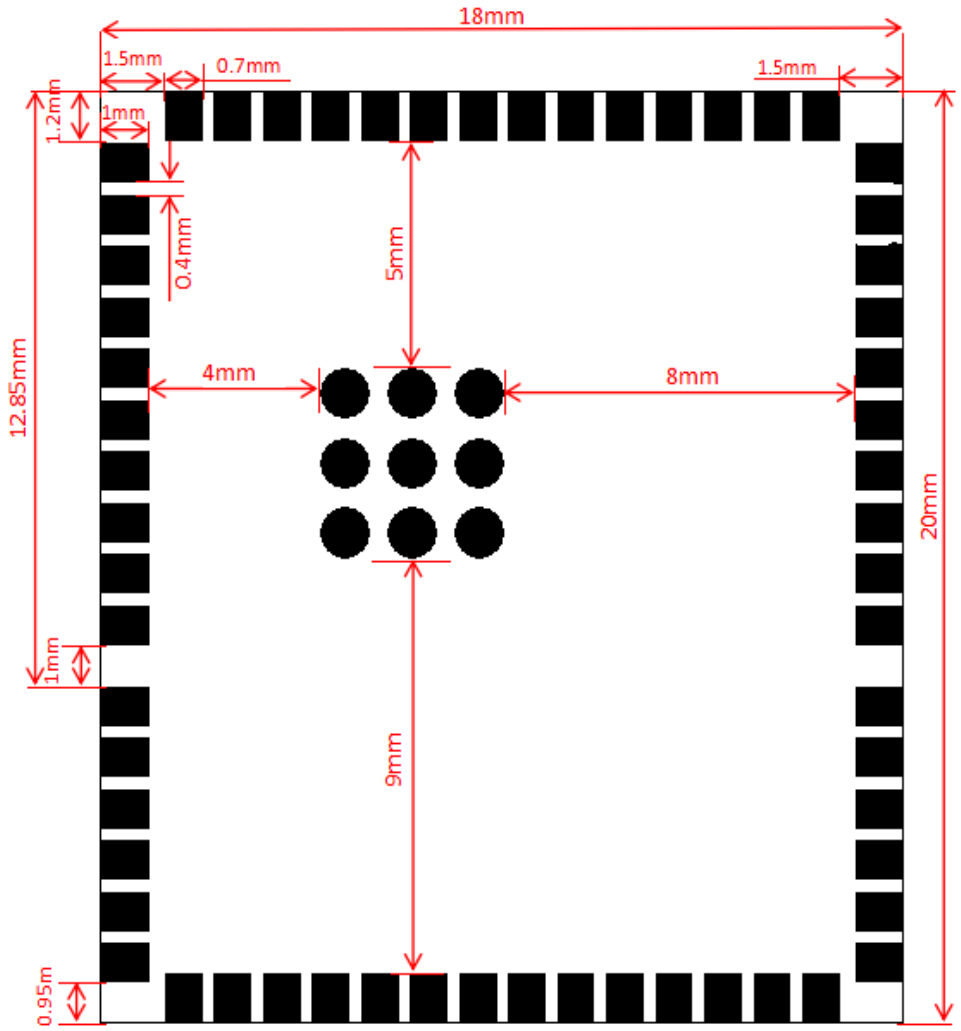
NOTE

All the values above are obtained in the lab environment. The RX sensitivity is obtained within 10% system error rate.

6 Mechanical Features

6.1 Dimensions

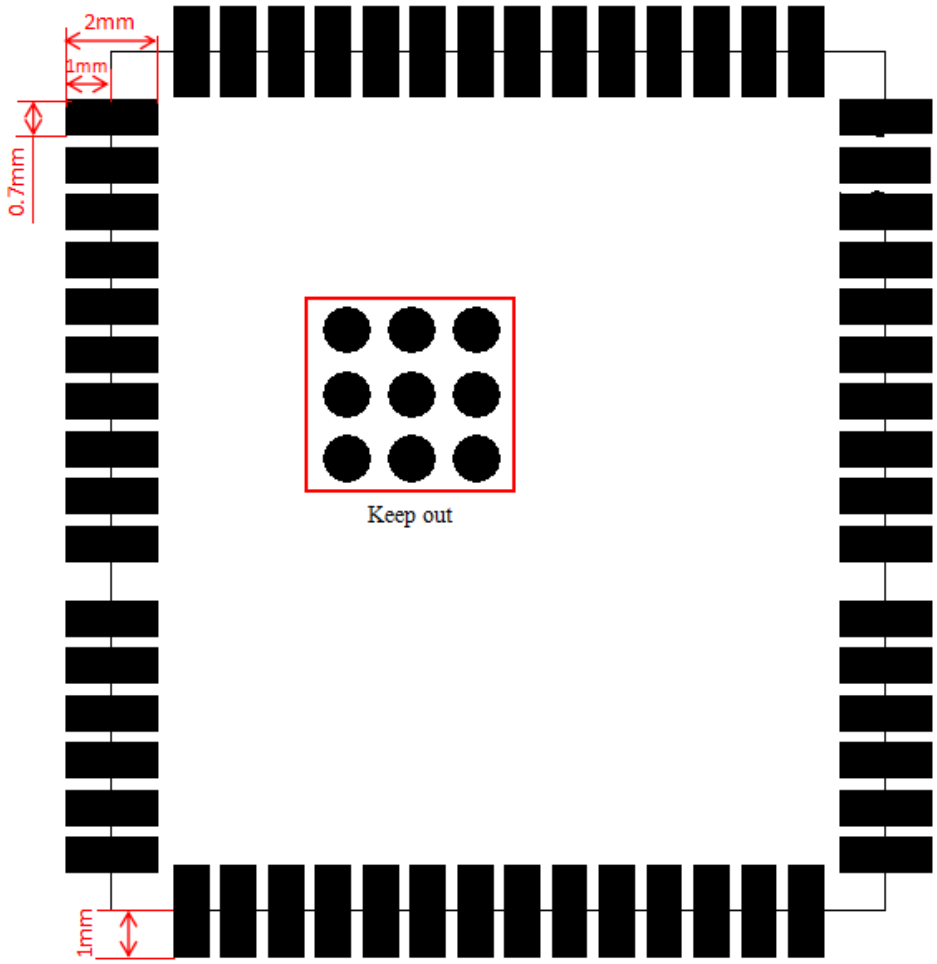
Figure 6-1 W30 dimensions(top view)



6.2 PCB Foot Print

LCC packaging is adopted to package the pins of the W30 module. Figure 6-2 shows the recommended PCB foot print (Unit: mm). Extend the pad around 1 mm to avoid short circuit caused by irregular flow of solder paste during the SMT process. Do not lay out any trace under the keepout area.

Figure 6-2 PCB foot print of W30 (top view)



7 Mounting and Packaging

7.1 Mounting the Module onto the Application Board

W30 is compatible with industrial standard reflow profile for lead-free SMT process. The reflow profile is process dependent, so the following recommendation is just a start point guideline:

- Make stencils with a thickness ranging from 0.12 mm to 0.15 mm, which can be adjusted according to the actual mounting conditions.
- The quality of the solder joint depends on the solder paste volume and the PCB flatness.
- Thin or long PCB might bend during SMT. So, use loading tools during the SMT and reflow soldering process to avoid poor solder joint caused by PCB bending.

For information about cautions in W30 storage and mounting, refer to *Neoway Module Reflow Manufacturing Recommendations*.

When manually desoldering the module, use heat guns with great opening, adjust the temperature to 250 degrees (depending on the type of the solder paste), and heat the module till the solder paste is melt. Then remove the module using tweezers. Do not shake the module in high temperatures while removing it. Otherwise, the components inside the module might get misplaced.

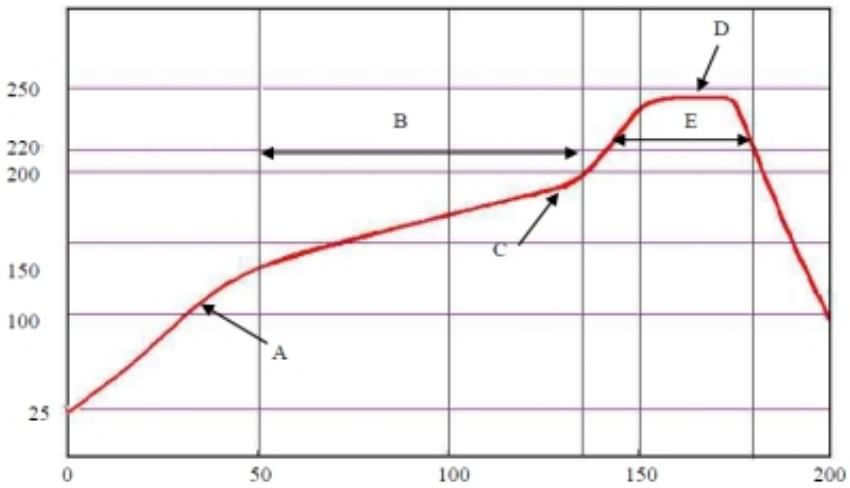
7.2 Package

W30 modules are packaged in sealed vacuum bags with dryer, humidity card, and tray on delivery to guarantee a long shelf life. Follow the same package method again in case of opened for any reasons.

If the module is exposed to air for more than 48 hours at conditions not worse than 30°C/60% RH, bake it at a temperature higher than 90 degree for more than 12 hours before SMT. Or, if the indication card shows humidity greater than 20%, the baking procedure is also required. Do not bake modules with the package tray directly.

8 SMT Furnace Temperature Curve

Figure 8-1 SMT furnace temperature curve



Technical parameters:

- Ramp up rate: 1 to 4 °C/sec

  Ramp down rate: -3 to -1 °C/sec
- Soaking zone: 150-180 °C, Time: 60-100 s
- Reflow zone: >220 °C, Time: 40-90 s
- Peak temperature: 235-250 °C

Do not use the kind of solder paste different from our module technique.

- The melting temperature of solder paste with lead is 35 °C lower than that of solder paste without lead. It is easy to cause faulty joints for BGA inside the module after second reflow soldering.
- When using only solder pastes with lead, please ensure that the reflow temperature is kept at 220 °C for more than 45 seconds and the peak temperature reaches 240 °C.

WARNING

Neoway will not provide warranty for heat-responsive element abnormalities caused by improper temperature control.

9 Abbreviations

WLAN	Wireless Local Area Networks
SDIO	Secure Digital Input and Output Card
PCM	Pulse Code Modulation
I2C	Inter-Integrated Circuit bus
I2S	Inter-IC Sound
UART	Universal asynchronous receiver-transmitter
ESD	Electronic Static Discharge
PCB	Printed Circuit Board
RF	Radio Frequency