ESP32-C3 Family

Datasheet

Ultra-Low-Power SoC with RISC-V Single-Core CPU

Supporting 2.4 GHz Wi-Fi and Bluetooth LE

Including:

ESP32-C3

ESP32-C3FN4

ESP32-C3FH4

Prerelease version 0.4
Espressif System

Product Overview

ESP32-C3 family is an ultra-low-power MCU-based SoC solution that supports 2.4 GHz Wi-Fi and Bluetooth® Low Energy (Bluetooth LE). It has:

- A complete Wi-Fi subsystem that complies with IEEE 802.11b/g/n protocol and supports Station, SoftAP, and SoftAP + Station modes
- A Bluetooth LE subsystem that supports features of Bluetooth 5 and Bluetooth mesh
- State-of-the-art power and RF performance
- 32-bit RISC-V single-core processor with a four-stage pipeline that operates at up to 160 MHz
- 400 KB of SRAM and 384 KB of ROM on the chip, and SPI, Dual SPI, Quad SPI, and QPI interfaces that allow connection to flash
- Reliable security features ensured by
  - Cryptographic hardware accelerators that support AES-128/256, Hash, RSA, HMAC, digital signature and secure boot
  - Random number generator
  - Permission control on accessing internal memory, external memory, and peripherals
  - External memory encryption and decryption
- Rich set of peripheral interfaces and GPIOs, ideal for various scenarios and complex applications

Block Diagram

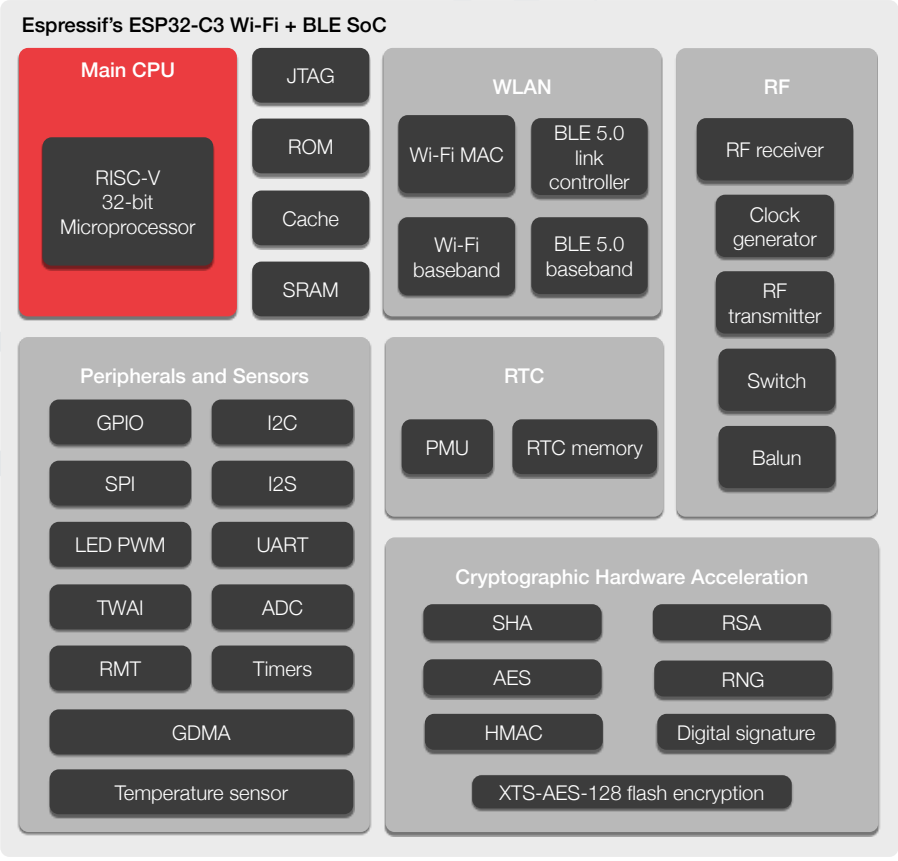

Figure 1: Block Diagram of ESP32-C3

Features

Wi-Fi

- IEEE 802.11 b/g/n-compliant
- Supports 20 MHz, 40 MHz bandwidth in 2.4 GHz band
- 1T1R mode with data rate up to 150 Mbps
- Wi-Fi Multimedia (WMM)
- TX/RX A-MPDU, RX A-MSDU
- Immediate Block ACK
- Fragmentation and defragmentation
- Automatic Beacon monitoring (hardware TSF)
- 4 × virtual Wi-Fi interfaces
- Simultaneous support for Infrastructure BSS in Station, SoftAP, or Station + SoftAP modes
  Note that when ESP32-C3 family scans in Station mode, the SoftAP channel will change along with the Station channel
- Antenna diversity
- 802.11mc FTM

Bluetooth

- Bluetooth LE: Bluetooth 5, Bluetooth mesh
- Speed: 125 Kbps, 500 Kbps, 1 Mbps, 2 Mbps
- Advertising extensions
- Multiple advertisement sets
- Channel selection algorithm #2

CPU and Memory

- 32-bit RISC-V single-core processor, up to 160 MHz
- 384 KB ROM
- 400 KB SRAM
- 8 KB SRAM in RTC
- SPI, Dual SPI, Quad SPI, and QPI interfaces that allow connection to multiple external flash

Advanced Peripheral Interfaces

- 22 × programmable GPIOs
- 2 × 12-bit SAR ADCs, up to 6 channels
- 1 × temperature sensor
- 3 × SPI
- 2 × UART
- 1 × I2C
- 1 × I2S
- Remote control peripheral, with 2 transmit channels and 2 receive channels
- LED PWM controller, up to 6 channels
- General DMA controller, with 3 transmit channels and 3 receive channels
- 1 × TWAI™ controller (compatible with ISO 11898-1)

Low Power Management

- Power Management Unit with five power modes

Security

- Secure boot
- Flash encryption
- 4096-bit OTP, up to 1792 bits for users
- Cryptographic hardware acceleration:
  - AES-128/256 (FIPS PUB 197)
- Permission Control
- SHA Accelerator (FIPS PUB 180-4)
- RSA Accelerator
- Random Number Generator (RNG)
- HMAC
- Digital signature

Applications (A Non-exhaustive List)

With ultra-low power consumption, ESP32-C3 family is an ideal choice for IoT devices in the following areas:

- Smart Home
  - Light control
  - Smart button
  - Smart plug
  - Indoor positioning
- Industrial Automation
  - Industrial robot
  - Mesh network
  - Human machine interface (HMI)
  - Industrial field bus
- Health Care
  - Health monitor
  - Baby monitor
- Consumer Electronics
  - Smart watch and bracelet
  - Over-the-top (OTT) devices
  - Wi-Fi and Bluetooth speaker
  - Logger toys and proximity sensing toys
- Smart Agriculture
  - Smart greenhouse
  - Smart irrigation
  - Agriculture robot
- Retail and Catering
  - POS machines
  - Service robot
- Audio Device
  - Internet music players
  - Live streaming devices
  - Internet radio players
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers

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1.1 Family Nomenclature

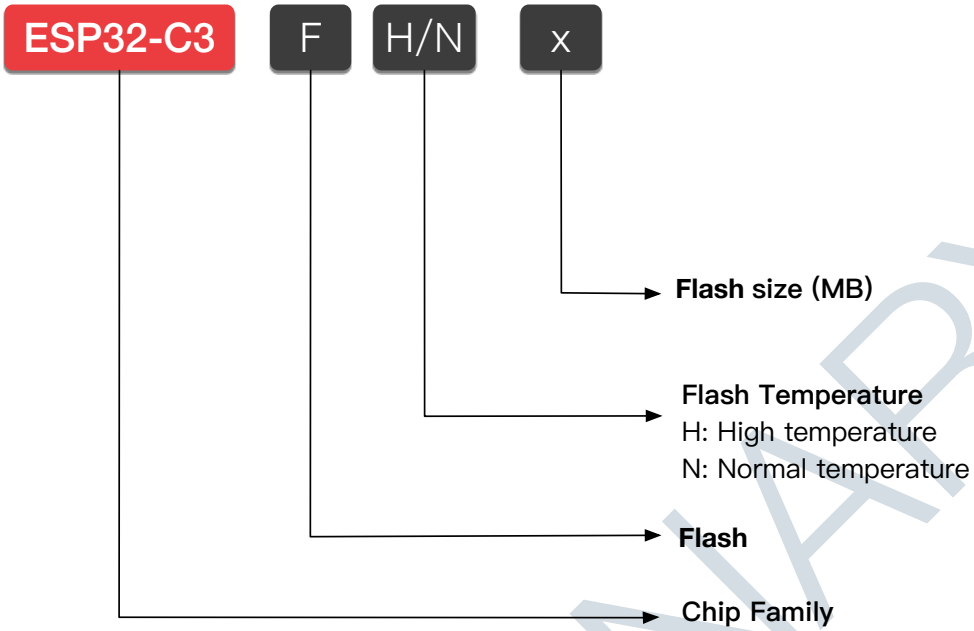

Figure 2: ESP32-C3 Family Nomenclature

1.2 Comparison

Table 1: ESP32-C3 Family Member Comparison

Ordering Code	Embedded Flash	Ambient Temperature (°C)	Package (mm)
ESP32-C3	No	–40 ~ 105	QFN32 (5*5)
ESP32-C3FN4	4 MB	–40 ~ 85	QFN32 (5*5)
ESP32-C3FH4	4 MB	–40 ~ 105	QFN32 (5*5)

2. Pin Definition

2.1 Pin Layout

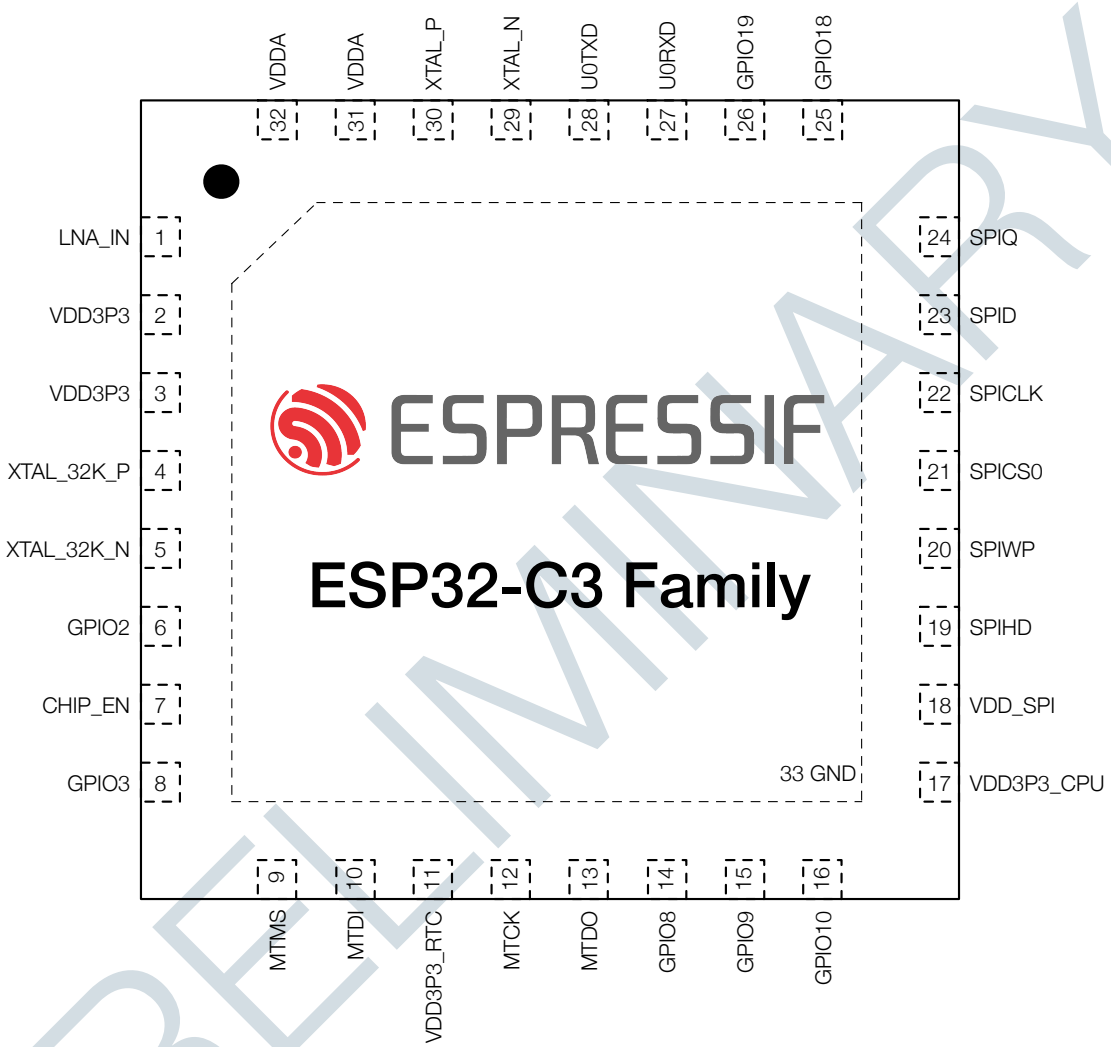

Figure 3: ESP32-C3 Pin Layout (Top View)

2.2 Pin Description

Table 2: Pin Description

Name	No.	Type	Power domain	Function
LNA_IN	1	I/O	—	RF input and output
VDD3P3	2	PA	—	Analog power supply
VDD3P3	3	PA	—	Analog power supply

Name	No.	Type	Power domain	Function
XTAL_32K_P	4	I/O/T	VDD3P3_RTC	GPIO0, ADC1_CH0, XTAL_32K_P
XTAL_32K_N	5	I/O/T	VDD3P3_RTC	GPIO1, ADC1_CH1, XTAL_32K_N
GPIO2	6	I/O/T	VDD3P3_RTC	GPIO2, ADC1_CH2, FSPIQ
CHIP_EN	7	I	VDD3P3_RTC	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the CHIP_PU pin floating.
GPIO3	8	I/O/T	VDD3P3_RTC	GPIO3, ADC1_CH3
MTMS	9	I/O/T	VDD3P3_RTC	GPIO4, ADC1_CH4, FSPIHD, MTMS
MTDI	10	I/O/T	VDD3P3_RTC	GPIO5, ADC2_CH0, FSPIWP MTDI
VDD3P3_RTC	11	PD	—	Input power supply for RTC
MTCK	12	I/O/T	VDD3P3_CPU	GPIO6, FSPICLK, MTCK
MTDO	13	I/O/T	VDD3P3_CPU	GPIO7, FSPID, MTDO
GPIO8	14	I/O/T	VDD3P3_CPU	GPIO8
GPIO9	15	I/O/T	VDD3P3_CPU	GPIO9
GPIO10	16	I/O/T	VDD3P3_CPU	GPIO10, FSPICS0
VDD3P3_CPU	17	PD	—	Input power supply for CPU IO
VDD_SPI	18	I/O/T/PD	VDD3P3_CPU	GPIO11, output power supply for flash
SPIHD	19	I/O/T	VDD3P3_CPU	GPIO12, SPIHD
SPIWP	20	I/O/T	VDD3P3_CPU	GPIO13, SPIWP
SPICS0	21	I/O/T	VDD3P3_CPU	GPIO14, SPICS0
SPICLK	22	I/O/T	VDD3P3_CPU	GPIO15, SPICLK
SPID	23	I/O/T	VDD3P3_CPU	GPIO16, SPID
SPIQ	24	I/O/T	VDD3P3_CPU	GPIO17, SPIQ
GPIO18	25	I/O/T	VDD3P3_CPU	GPIO18
GPIO19	26	I/O/T	VDD3P3_CPU	GPIO19
U0RXD	27	I/O/T	VDD3P3_CPU	GPIO20, U0RXD
U0TXD	28	I/O/T	VDD3P3_CPU	GPIO21, U0TXD
XTAL_N	29	—	—	External crystal output
XTAL_P	30	—	—	External crystal input
VDDA	31	PA	—	Analog power supply
VDDA	32	PA	—	Analog power supply
GND	33	G	—	Ground

Note:

1. P: power pin; I: input; O: output; T: high impedance.
2. VDD_SPI, SPIHD, SPIWP, SPICS0, SPICLK, SPIQ, and SPID pins of ESP32-C3FN4 and ESP32-C3FH4 are used for connecting the embedded flash, and are not recommended for other uses.
3. For the data port connection between ESP32-C3 family and external flash please refer to section 3.4.2.
4. The pin function in this table refers only to some fixed settings and do not cover all cases for signals that can be input and output through the GPIO matrix. For more information on the GPIO matrix, please refer to ESP32-C3 Technical Reference Manual.

2.3 Power Scheme

Digital pins of ESP32-C3 family are divided into four different power domains:

- VDD3P3_CPU
- VDD_SPI
- VDD3P3_RTC

VDD3P3_CPU is the input power supply for CPU.

VDD_SPI can be an input power supply or an output power supply.

VDD3P3_RTC is the input power supply for RTC analog domain and CPU.

The power scheme diagram is shown in Figure 4.

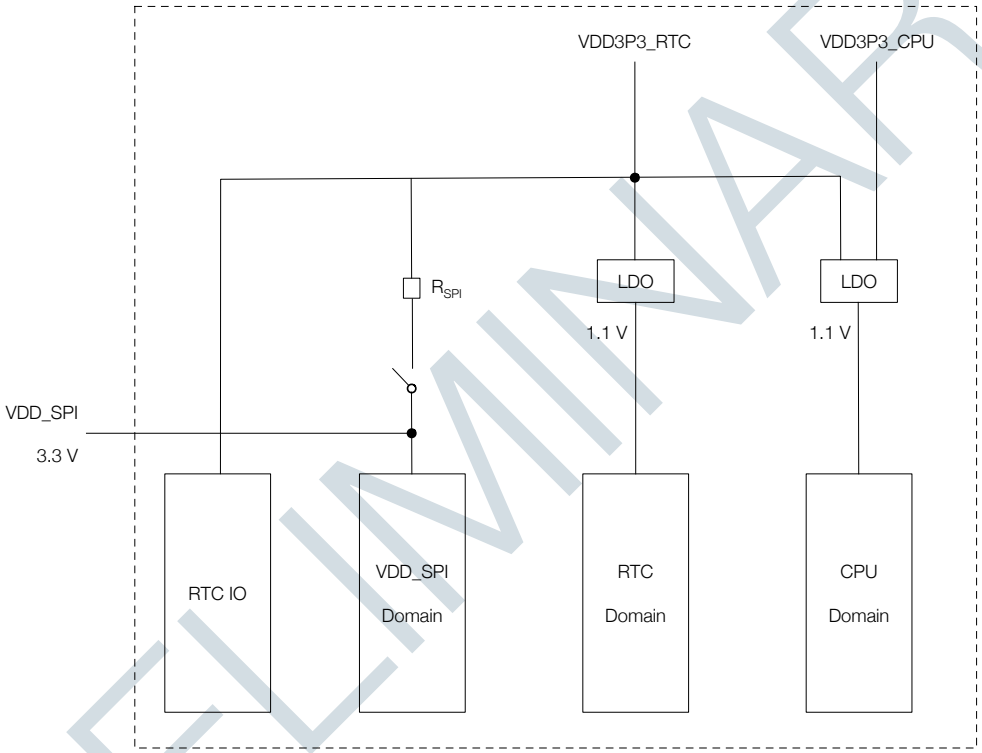

Figure 4: ESP32-C3 Family Power Scheme

When working as an output power supply, VDD_SPI can be powered by VDD3P3_RTC via R_{SPI} (nominal 3.3 V). VDD_SPI can be powered off via software to minimize the current leakage of flash in Deep-sleep mode.

2.4 Strapping Pins

ESP32-C3 family has three strapping pins:

- GPIO8
- GPIO9
- GPIO10

Software can read the values of corresponding bits from the register "GPIO_STRAPPING".

During the chip's system reset (power-on-reset, RTC watchdog reset, brownout reset, analog super watchdog reset, and crystal clock glitch detection reset), the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down.

By default GPIO9 is connected to the chip's internal pull-up. Consequently, if GPIO9 is unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine its default input level.

To change the strapping bit values, you can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32-C3.

After reset, the strapping pins work as normal-function pins.

Refer to Table 3 for a detailed boot-mode configuration of the strapping pins.

Table 3: Strapping Pins

Booting Mode [1]			
Pin	Default	SPI Boot	Download Boot
GPIO8	N/A	Any value	1
GPIO9	Pull-up	1	0
Enabling/Disabling ROM Code Print During Booting			
Pin	Default	Functionality	
GPIO8	N/A	When the value of eFuse bit UART_PRINT_CONTROL is 0, print is enabled and not controlled by GPIO8. 1, if GPIO8 is 0, print is enabled; if GPIO8 is 1, it is disabled. 2, if GPIO8 is 0, print is disabled; if GPIO8 is 1, it is enabled. 3, print is disabled and not controlled by GPIO8.	
Controlling JTAG Signal Source During Booting			
Pin	Default	Functionality	
GPIO10	N/A	When the value of eFuse bit EFUSE_JTAG_SEL_ENABLE is 0, JTAG signals cannot be used. 1, if GPIO10 is 0, JTAG signals come from chip pins; if GPIO10 is 1, JTAG signals cannot be used.	

Note:

1. The strapping combination of GPIO8 = 0 and GPIO9 = 0 is invalid and will trigger unexpected behavior.

3. Functional Description

3.1 CPU and Memory

3.1.1 CPU

ESP32-C3 family has a low-power 32-bit RISC-V single-core microprocessor with the following features:

- four-stage pipeline that supports a clock frequency of up to 160 MHz
- RV32IMC ISA
- 32-bit multiplier and 32-bit divider
- up to 32 vectored interrupts at seven priority levels
- up to 8 hardware breakpoints/watchpoints
- up to 16 PMP regions
- JTAG for debugging

3.1.2 Internal Memory

ESP32-C3's internal memory includes:

- **384 KB of ROM**: for booting and core functions
- **400 KB of on-chip SRAM**: for data and instructions
- **RTC memory**: 8 KB of SRAM that can be accessed by the main CPU. It can retain data in Deep-sleep mode
- **4 Kbit of eFuse**: 1792 bits are reserved for user data, such as encryption key and device ID.

3.1.3 External Flash

ESP32-C3 family supports SPI, Dual SPI, Quad SPI, and QPI interfaces that allow connection to multiple external flash.

CPU's instruction memory space and read-only data memory space can map into external flash of ESP32-C3, whose size can be 16 MB at most. ESP32-C3 family supports hardware encryption/decryption based on XTS-AES to protect developers' programs and data in flash.

Through high-speed caches, ESP32-C3 family can support at a time up to:

- 8 MB of instruction memory space which can map into flash as individual blocks of 64 KB. 8-bit, 16-bit and 32-bit reads are supported.
- 8 MB of data memory space which can map into flash as individual blocks of 64 KB. 8-bit, 16-bit and 32-bit reads are supported.

Note:
After ESP32-C3 family is initialized, software can customize the mapping of external RAM into the CPU address space.

3.1.4 Address Mapping Structure

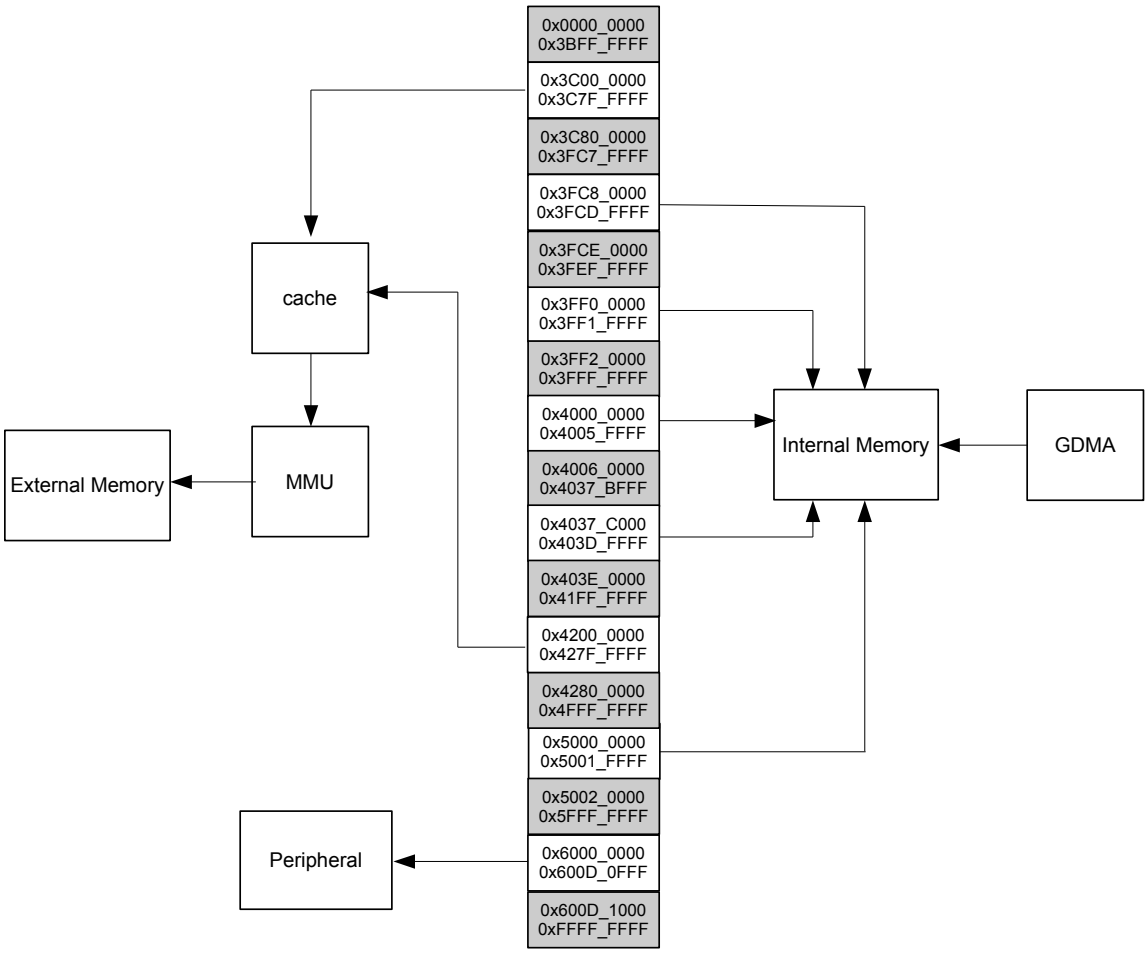

Figure 5: Address Mapping Structure

Note:
The memory space with gray background is not available to users.

3.1.5 Cache

ESP32-C3 family has an eight-way set associative cache. This cache is read-only and has the following features:

- size: 16 KB
- block size: 32 bytes
- pre-load function
- lock function
- critical word first and early restart

3.2 System Clocks

3.2.1 CPU Clock

The CPU clock has three possible sources:

- external main crystal clock
- internal 20 MHz oscillator
- PLL clock

The application can select the clock source from the three clocks above. The selected clock source drives the CPU clock directly, or after division, depending on the application.

3.2.2 RTC Clock

The RTC slow clock is used for RTC counter, RTC watchdog and low-power controller. It has three possible sources:

- external low-speed (32 kHz) crystal clock
- internal RC oscillator (typically about 150 kHz, and adjustable)
- internal 78.125 kHz clock (derived from the internal 20 MHz oscillator divided by 256)

The RTC fast clock is used for RTC peripherals and sensor controllers. It has two possible sources:

- external main crystal clock divided by 2
- internal 20 MHz oscillator

3.3 Analog Peripherals

3.3.1 Analog-to-Digital Converter (ADC)

ESP32-C3 family integrates two 12-bit SAR ADCs and supports measurements on 6 channels (analog-enabled pins).

3.3.2 Temperature Sensor

The temperature sensor generates a voltage that varies with temperature. The voltage is internally converted via an ADC into a digital value.

The temperature sensor has a range of –20 °C to 110 °C. It is designed primarily to sense the temperature changes inside the chip. The temperature value depends on factors like microcontroller clock frequency or I/O load. Generally, the chip's internal temperature is higher than the ambient temperature.

3.4 Digital Peripherals

3.4.1 General Purpose Input / Output Interface (GPIO)

ESP32-C3 family has 22 GPIO pins which can be assigned various functions by configuring corresponding registers. Besides digital signals, some GPIOs can be also used for analog functions, such as ADC.

All GPIOs have selectable internal pull-up or pull-down, or can be set to high impedance. When these GPIOs are configured as an input, the input value can be read by software through the register. Input GPIOs can also be set to generate edge-triggered or level-triggered CPU interrupts. All digital IO pins are bi-directional, non-inverting

and tristate, including input and output buffers with tristate control. These pins can be multiplexed with other functions, such as the UART, SPI, etc. For low-power operations, the GPIOs can be set to holding state.

The IO MUX and the GPIO matrix are used to route signals from peripherals to GPIO pads. Together they provide highly configurable I/O. Using GPIO Matrix, peripheral input signals can be configured from any IO pads while peripheral output signals can be configured to any IO pads.

3.4.2 Serial Peripheral Interface (SPI)

ESP32-C3 family features three SPI interfaces (SPI0, SPI1, and SPI2). SPI0 and SPI1 can only be configured to operate in SPI memory mode, while SPI2 can be configured to operate in both SPI memory and general-purpose SPI modes.

- **SPI Memory mode**

  In SPI memory mode, SPI0, SPI1 and SPI2 interface with external SPI memory. Data is transferred in bytes. Up to four-line STR reads and writes are supported. The clock frequency is configurable to a maximum of 120 MHz in STR mode.

- **SPI2 General-purpose SPI (GP-SPI) mode**

  When SPI2 acts as a general-purpose SPI, it can operate in master and slave modes. SPI2 supports two-line full-duplex communication and single-/two-/four-line half-duplex communication in both master and slave modes. The host's clock frequency is configurable. Data is transferred in bytes. The clock polarity (CPOL) and phase (CPHA) are also configurable. The SPI2 interface can connect to GDMA.

  - In two-line full-duplex mode, the clock frequency of host and slave is configurable to 80 MHz at most. Four modes of SPI transfer format are supported.
  - In single-/two-/four-line half-duplex mode, the host's clock frequency is configurable to 80 MHz at most and the four modes of SPI transfer format are supported.
  - In single-/two-/four-line half-duplex mode, the slave's clock frequency is configurable to 60 MHz at most, and the four modes of SPI transfer format are also supported.

In most cases, the data port connection between ESP32-C3 family and external flash is as follows:

Table 4: Connection Between ESP32-C3 Family and External Flash

	SPI single-line mode	SPI two-line mode	SPI four-line mode
SPID (SPID)	DI	IO0	IO0
SPIQ (SPIQ)	DO	IO1	IO1
SPIWP (SPIWP)	WP#	N/A	IO2
SPIHD (SPIHD)	HOLD#	N/A	IO3

3.4.3 Universal Asynchronous Receiver Transmitter (UART)

ESP32-C3 family has two UART interfaces, i.e. UART0 and UART1, which support IrDA and asynchronous communication (RS232 and RS485) at a speed of up to 5 Mbps. The UART controller provides hardware flow control (CTS and RTS signals) and software flow control (XON and XOFF). Both UART interfaces connect to GDMA via UHCI0, and can be accessed by the GDMA controller or directly by the CPU.

3.4.4 I2C Interface

ESP32-C3 family has an I2C bus interface which is used for I2C master mode or slave mode, depending on the user's configuration. The I2C interface supports:

- standard mode (100 Kbit/s)
- fast mode (400 Kbit/s)
- up to 800 Kbit/s (constrained by SCL and SDA pull-up strength)
- 7-bit and 10-bit addressing mode
- double addressing mode
- 7-bit broadcast address

Users can configure instruction registers to control the I2C interface for more flexibility.

3.4.5 I2S Interface

ESP32-C3 family includes a standard I2S interface. This interface can operate as a master or a slave in full-duplex mode or half-duplex mode, and can be configured for 8-bit, 16-bit, 24-bit, or 32-bit serial communication. BCK clock frequency, from 10 kHz up to 40 MHz, is supported.

The I2S interface supports TDM PCM, TDM MSB alignment, TDM standard, and PDM TX interface. It connects to the GDMA controller.

3.4.6 Remote Control Peripheral

The Remote Control Peripheral (RMT) supports two channels of infrared remote transmission and two channels of infrared remote reception. By controlling pulse waveform through software, it supports various infrared and other single wire protocols. All four channels share a 192 × 32-bit memory block to store transmit or receive waveform.

3.4.7 LED PWM Controller

The LED PWM controller can generate independent digital waveform on six channels. The LED PWM controller:

- can generate digital waveform with configurable periods and duty cycle. The accuracy of duty cycle can be up to 18 bits.
- has multiple clock sources, including APB clock and external main crystal clock.
- can operate when the CPU is in Light-sleep mode.
- supports gradual increase or decrease of duty cycle, which is useful for the LED RGB color-gradient generator.

3.4.8 General DMA Controller

ESP32-C3 family has a general DMA controller (GDMA) with six independent channels, i.e. three transmit channels and three receive channels. These six channels are shared by peripherals with DMA feature, and support dynamic priority.

The GDMA controller controls data transfer using linked lists. It allows peripheral-to-memory and memory-to-memory data transfer at a high speed. All channels can access internal RAM.

Peripherals on ESP32-C3 family with DMA feature are SPI2, UHCI0, I2S, AES, SHA, and ADC.

3.4.9 TWAI™ Controller

ESP32-C3 family has a TWAI™ controller with the following features:

- compatible with ISO 11898-1 protocol

- standard frame format (11-bit ID) and extended frame format (29-bit ID)
- bit rates from 1 Kbit/s to 1 Mbit/s
- multiple modes of operation: Normal, Listen Only, and Self-Test (no acknowledgment required)
- 64-byte receive FIFO
- acceptance filter (single and dual filter modes)
- error detection and handling: error counters, configurable error interrupt threshold, error code capture, arbitration lost capture

3.5 Radio and Wi-Fi

The ESP32-C3 family radio consists of the following blocks:

- 2.4 GHz receiver
- 2.4 GHz transmitter
- bias and regulators
- balun and transmit-receive switch
- clock generator

3.5.1 2.4 GHz Receiver

The 2.4 GHz receiver demodulates the 2.4 GHz RF signal to quadrature baseband signals and converts them to the digital domain with two high-resolution, high-speed ADCs. To adapt to varying signal channel conditions, ESP32-C3 family integrates RF filters, Automatic Gain Control (AGC), DC offset cancelation circuits, and baseband filters.

3.5.2 2.4 GHz Transmitter

The 2.4 GHz transmitter modulates the quadrature baseband signals to the 2.4 GHz RF signal, and drives the antenna with a high-powered CMOS power amplifier. The use of digital calibration further improves the linearity of the power amplifier.

Additional calibrations are integrated to cancel any radio imperfections, such as:

- carrier leakage
- I/Q amplitude/phase matching
- baseband nonlinearities
- RF nonlinearities
- antenna matching

These built-in calibration routines reduce the cost, time, and specialized equipment required for product testing.

3.5.3 Clock Generator

The clock generator produces quadrature clock signals of 2.4 GHz for both the receiver and the transmitter. All components of the clock generator are integrated into the chip, including inductors, varactors, filters, regulators and dividers.

The clock generator has built-in calibration and self-test circuits. Quadrature clock phases and phase noise are optimized on chip with patented calibration algorithms which ensure the best performance of the receiver and the transmitter.

3.5.4 Wi-Fi Radio and Baseband

The ESP32-C3 family Wi-Fi radio and baseband support the following features:

- 802.11b/g/n
- 802.11n MCS0-7 that supports 20 MHz and 40 MHz bandwidth
- 802.11n MCS32
- 802.11n 0.4 μs guard interval
- data rate up to 150 Mbps
- RX STBC (single spatial stream)
- adjustable transmitting power
- antenna diversity
  ESP32-C3 family supports antenna diversity with an external RF switch. This switch is controlled by one or more GPIOs, and used to select the best antenna to minimize the effects of channel imperfections.

3.5.5 Wi-Fi MAC

ESP32-C3 family implements the full 802.11 b/g/n Wi-Fi MAC protocol. It supports the Basic Service Set (BSS) STA and SoftAP operations under the Distributed Control Function (DCF). Power management is handled automatically with minimal host interaction to minimize the active duty period.

The ESP32-C3 family Wi-Fi MAC applies the following low-level protocol functions automatically:

- 4 × virtual Wi-Fi interfaces
- simultaneous Infrastructure BSS Station mode, SoftAP mode, and Station + SoftAP mode
- RTS protection, CTS protection, Immediate Block ACK
- fragmentation and defragmentation
- TX/RX A-MPDU, RX A-MSDU
- TXOP
- WMM
- GCMP, CCMP, TKIP, WAPI, WEP, and BIP
- automatic beacon monitoring (hardware TSF)
- 802.11mc FTM

3.5.6 Networking Features

Users are provided with libraries for TCP/IP networking, ESP-WIFI-MESH networking, and other networking protocols over Wi-Fi. TLS 1.0, 1.1 and 1.2 is also supported.

3.6 Bluetooth LE

ESP32-C3 family includes a Bluetooth Low Energy subsystem that integrates a hardware link layer controller, an RF/modem block and a feature-rich software protocol stack. It supports the core features of Bluetooth 5 and Bluetooth mesh.

3.6.1 Bluetooth LE Radio and PHY

Bluetooth Low Energy radio and PHY in ESP32-C3 family support:

- 1 Mbps PHY
- 2 Mbps PHY for high transmission speed and high data throughput
- coded PHY for high RX sensitivity and long range (125 Kbps and 500 Kbps)
- listen before talk (LBT), implemented in hardware
- antenna diversity with an external RF switch. This switch is controlled by one or more GPIOs, and used to select the best antenna to minimize the effects of channel imperfections

3.6.2 Bluetooth LE Link Layer Controller

Bluetooth Low Energy Link Layer Controller in ESP32-C3 family support:

- LE advertising extensions, to enhance broadcasting capacity and broadcast more intelligent data
- multiple advertisement sets
- simultaneous advertising and scanning
- multiple connections in simultaneous central and peripheral roles
- adaptive frequency hopping and channel assessment
- LE channel selection algorithm #2
- connection parameter update
- high duty cycle non-connectable advertising
- LE privacy 1.2
- LE data packet length extension
- link layer extended scanner filter policies
- low duty cycle directed advertising
- link layer encryption
- LE Ping

3.7 Low Power Management

With the use of advanced power-management technologies, ESP32-C3 family can switch between different power modes.

- Active mode: CPU and chip radio are powered on. The chip can receive, transmit, or listen.
- Modem-sleep mode: The CPU is operational and the clock speed can be reduced. Wi-Fi base band, Bluetooth LE base band, and radio are disabled, but Wi-Fi and Bluetooth LE connection can remain active.

- Light-sleep mode: The CPU is paused. Any wake-up events (MAC, host, RTC timer, or external interrupts) will wake up the chip. Wi-Fi and Bluetooth LE connection can remain active.
- Deep-sleep mode: CPU and most peripherals are powered down. Only the RTC memory is powered on. Wi-Fi connection data are stored in the RTC memory.
- Hibernation mode: The internal 20-MHz oscillator is disabled. Only one RTC timer on the slow clock is active. The RTC timer or the RTC GPIOs can wake up the chip from the Hibernation mode.

3.8 Timers

3.8.1 General Purpose Timers

ESP32-C3 family is embedded with two 54-bit general-purpose timers, which are based on 16-bit prescalers and 54-bit auto-reload-capable up/down-timers.

The timers' features are summarized as follows:

- a 16-bit clock prescaler, from 1 to 65536
- a 54-bit time-base counter programmable to be incrementing or decrementing
- able to read real-time value of the time-base counter
- halting and resuming the time-base counter
- programmable alarm generation
- level interrupt generation

3.8.2 System Timer

ESP32-C3 family integrates a 52-bit system timer, which has two 52-bit counters and three comparators. The system timer has the following features:

- counters with a fixed clock frequency of 16 MHz
- three types of independent interrupts generated according to alarm value
- two alarm modes: target mode and period mode
- 52-bit target alarm value and 26-bit periodic alarm value
- automatic reload of counter value
- counters can be stalled if the CPU is stalled or in OCD mode

3.8.3 Watchdog Timers

The ESP32-C3 family contains three watchdog timers: one in each of the two timer groups (called Main System Watchdog Timers, or MWDT) and one in the RTC module (called the RTC Watchdog Timer, or RWDT).

During the flash boot process, RWDT and the MWDT in timer group 0 (TIMG0) are enabled automatically in order to detect and recover from booting errors.

Watchdog timers have the following features:

- four stages, each with a programmable timeout value. Each stage can be configured, enabled and disabled separately
- interrupt, CPU reset, or core reset for MWDT upon expiry of each stage; interrupt, CPU reset, core reset, or system reset for RWDT upon expiry of each stage

- 32-bit expiry counter
- write protection, to prevent RWDT and MWDT configuration from being altered inadvertently
- flash boot protection
  If the boot process from an SPI flash does not complete within a predetermined period of time, the watchdog will reboot the entire main system.

3.9 Cryptographic Hardware Accelerators

ESP32-C3 family is equipped with hardware accelerators of general algorithms, such as AES-128/AES-256 (FIPS PUB 197), ECB/CBC/OFB/CFB/CTR (NIST SP 800-38A), SHA1/SHA224/SHA256 (FIPS PUB 180-4), RSA3072, and ECC. The chip also supports independent arithmetic, such as Big Integer Multiplication and Big Integer Modular Multiplication. The maximum operation length for RSA and Big Integer Modular Multiplication is 3072 bits. The maximum factor length for Big Integer Multiplication is 1536 bits.

3.10 Physical Security Features

- transparent external flash encryption (AES-XTS algorithm) with software inaccessible key prevents unauthorized readout of user application code or data.
- secure boot feature uses a hardware root of trust to ensure only signed firmware (with RSA-PSS signature) can be booted.
- HMAC module can use a software inaccessible MAC key to generate MAC signatures for identity verification and other purposes.
- Digital Signature module can use a software inaccessible secure key to generate RSA signatures for identity verification.
- World Controller provides two running environments for software. All hardware and software resources are sorted to two groups, and placed in either secure or general world. The secure world cannot be accessed by hardware in the general world, thus establishing a security boundary.

3.11 Peripheral Pin Configurations

Table 5: Peripheral Pin Configurations

Interface	Signal	Pin	Function
ADC	ADC1_CH0	GPIO0	Two 12-bit SAR ADCs
	ADC1_CH1	GPIO1	
	ADC1_CH2	GPIO2	
	ADC1_CH3	GPIO3	
	ADC2_CH0	GPIO5	
JTAG	MTDI	MTDI	JTAG for software debugging
	MTCK	MTCK	
	MTMS	MTMS	
	MTDO	MTDO	

Interface	Signal	Pin	Function
UART	U0RXD_in	Any GPIO pins	Two UART devices with hardware flow control and GDMA
	U0CTS_in		
	U0DSR_in		
	U0TXD_out		
	U0RTS_out		
	U0DTR_out		
	U1RXD_in		
	U1CTS_in		
	U1DSR_in		
	U1TXD_out		
	U1RTS_out		
	U1DTR_out		
I2C	I2CEXT0_SCL_in	Any GPIO pins	One I2C device in slave or master mode
	I2CEXT0_SDA_in		
	I2CEXT1_SCL_in		
	I2CEXT1_SDA_in		
	I2CEXT0_SCL_out		
	I2CEXT0_SDA_out		
	I2CEXT1_SCL_out		
	I2CEXT1_SDA_out		
LED PWM	ledc_ls_sig_out0~5	Any GPIO pins	Six independent channels. 80 MHz clock, RTC clock or XTAL clock. Duty cycle accuracy: 14 bits
I2S	I2S0O_BCK_in	Any GPIO pins	Stereo input and output from/to the audiocodec
	I2S_MCLK_in		
	I2SO_WS_in		
	I2SI_SD_in		
	I2SI_BCK_in		
	I2SI_WS_in		
	I2SO_BCK_out		
	I2S_MCLK_out		
	I2SO_WS_out		
	I2SO_SD_out		
	I2SI_BCK_out		
	I2SI_WS_out		
	I2SO_SD1_out		
Remote Control Peripheral	RMT_SIG_IN0~1	Any GPIO pins	Two channels for an IR transceiver of various waveforms
	RMT_SIG_OUT0~1		
SPI0/1	SPICLK_out_mux	SPICLK	Support Standard SPI, Dual SPI, Quad SPI, and QPI that allow connection to external flash.
	SPICS0_out	SPICS0	
	SPICS1_out	SPICS1	
	SPID_in/_out	SPID	
	SPIQ_in/_out	SPIQ	
	SPIWP_in/_out	SPIWP	
	SPIHD_in/_out	SPIHD	

Interface	Signal	Pin	Function
SPI2	FSPICLK_in/_out_mux	Any GPIO pins	• Master mode and slave mode of SPI, Dual SPI, Quad SPI, and QPI; • Connection to external flash, RAM, and other SPI devices; • Four modes of SPI transfer format; • Configurable SPI frequency; • 64-byte FIFO or GDMA buffer.
	FSPICS0_in/_out		
	FSPICS1~5_out		
	FSPID_in/_out		
	FSPIQ_in/_out		
	FSPIWP_in/_out		
	FSPIHD_in/_out		

Revision History

Date	Version	Release notes
2020-11-27	V0.4	Preliminary version.

Solutions, Documentation and Legal Information

Must-Read Documents

- *ESP-IDF Programming Guide*
- *Espressif Product Ordering Information*
- Certificates
- Notification Subscription

Sales and Technical Support

- Sales Questions
- Technical Inquiries
- Get Samples

Developer Zone

- ESP32 Forum
- GitHub
- Courses
- Videos

Products

- SoCs
- Modules
- DevKits

Must-Have Resources

- SDKs and Demos
- APPs
- Tools
- AT

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